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Power Efficient Design of DisplayPort (7.0) Using Low-voltage differential signaling IO Standard Via UltraScale Field Programming Gate Arrays

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Abstract— **The DisplayPort (7.0) provides transection of serial-digital video displays, it has TX and RX Controllers along with pixel video interface, with streaming line rate of maximum 5.4 Gb/s. However, the limitation of DisplayPort (7.0) are detected in terms of power consumption. It has been reported that DisplayPort (7.0) consumes a massive power as it works on high frequency 1.62 GHz for high resolution video processing using HDMI Port. It is also stated that at full brightness the DisplayPort (7.0) consumes 49.0 W Therefore for power efficient DisplayPort (7.0) the full brightness power of DisplayPort (7.0) need be reduced. In this paper, a power efficient design for DisplayPort (7.0) is proposed using LVDS IO Standard. The proposed design is tested for different frequencies; 500 MHz, 700 MHz, 1.0 GHz, and 1.6 GHz. The design is implemented using vhdl in UltraScale FPGA. It is determined the designed vhdl based design of DisplayPort (7.0) can reduced 92% using LVDS IO Standard for all frequencies; 500 MHz, 700 MHz, 1.0 GHz, and 1.6 GHz, compared to vhdl based design of DisplayPort (7.0) without using IO Standard. The proposed design of vhdl based design of DisplayPort (7.0) using LVDS IO Standard offers no power consumption for DisplayPort (7.0) in standby mode. The vhdl based design of DisplayPort (7.0) using LVDS IO Standard will be helpful to process the high resolution video at low power consumption.**

Keywords- *Power Consumption, DisplayPort (7.0), IO Standard, UltraScale Field Prograaming Gate Array.*

I. INTRODUCTION

The Xilinx DisplayPort (7.0) is an interconnect protocol that is aimed to provide the transmission and reception of serial-digital video for consumer and professional displays [1]. DisplayPort offers a high-speed serial interface maintained by chipsets, display controllers, and monitors. DisplayPort substitutes Video Graphic Adaptor (VGA) [1]. DisplayPort delivers the HDMI output that provides higher resolution, high frame rate display. DisplayPort has TX and RX Controllers along with pixel video interface, audio and video controller, and data streaming line rate of maximum 5.4 Gb/s [1]. However, the limitation of DisplayPort (7.0) are observed in terms of power consumption. For DisplayPort (7.0) consumes a massive power as it works on high frequency 1.62 GHz for providing the maximum line rate of 5.4 Gb/s [1]. It is defined that DisplayPort (7.0) offers the high resolution video processing using HDMI Port. The power consumption of DisplayPort (7.0) is also increasing, when the high resolution video is processed [2]. It is also reported in [2] that at full brightness the DisplayPort (7.0) consumes 49.0 W and 0.0 W in Standby mode. The standby model power consumption is almost negligible but at full brightness the DisplayPort (7.0) the power consumption is extremely high. Therefore for power efficient DisplayPort (7.0) the full brightness power of DisplayPort (7.0) need be reduced. There are

several techniques are utilized in order to control or reduce the power consumption of different devices such as; optical transmitter [3], energy efficient laser driver [4], Ethernet [5], filters [6]. These techniques include; these techniques include; clock gating, voltage scaling [7], variable frequency and etc. However, each techniques has its own advantages and disadvantages. It has been demonstrated in [8-9] that for different variation in suitable IO Standard the power consumption of device can be reduced depend upon the core voltage of Field Programming Gate Array (FPGA), operating voltage of the device and IO Standard voltage selected for particular device. There are various IO Standards are available on different FPGA. The selection of particular IO Standard depends upon the particular device for which it is configured. For DisplayPort, the high speed serial communication is required. In this concern, the most suitable IO Standard for DisplayPort is Low-voltage differential signaling (LVDS) IO Standard. Low-voltage differential signaling (LVDS) is also named as TIA/EIA-644. This TIA/EIA-644 is a technical standard that defines the electrical characteristics of the serial communications protocol with differential characteristics. LVDS functions at low power and offers high-speed interface for various applications [10]. The LVDS I/Os are designed to fulfil with the EIA/TIA specifications for signaling system. The LVDS offers the internal differential termination feature. The LVDS IO Standard requires a VCCO to be 1.8V for outputs. The LVDS IO Standard is categorized as High Performance (HP) Io Standard. The LVDS is configured with another IO standard that is LVDS_ 25 IO Standard. LVDS_ 25 IO Standard operates at 2.5 V [11]. In this paper, the power efficient design is demonstrated for DisplayPort (7.0) for high frequency operation using Low-voltage differential signaling (LVDS) IO Standard via UltraScale Field Programming Gate Array. In the next section, the methodology of designing the power efficient design of DisplayPort (7.0) is discussed.

II. METHODOLOGY

The power efficient design of DisplayPort (7.0) for high frequency using LVDS IO Standard is designed using different design stages as demonstrated in Figure 1.

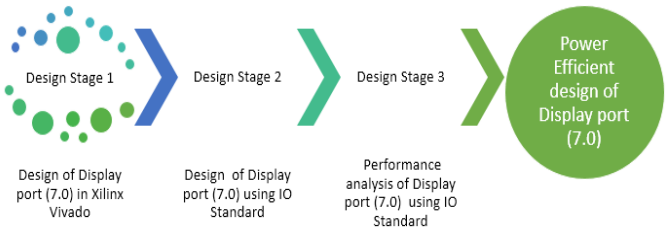

Figure 1. Design stages for designing the power efficient design of DisplayPort (7.0)

It is demonstrated in Figure 1 that in the first design stage, the DisplayPort (7.0) is designed using Vivado design suite via vhdl coding by defining the different parameters and configuration of transmitter and receiver. In the second design stage, the vhdl based DisplayPort (7.0) is designed using LVDS IO Standard. The LVDS IO Standard is selected because DisplayPort (7.0) need a high speed serial bus for its processing. In the third design stage, the power consumption of the vhdl based DisplayPort (7.0) using LVDS IO Standard is tested for different high frequencies and power consumption comparison is also demonstrated between DisplayPort (7.0) and LVDS based DisplayPort (7.0) in order to analyze the performance of the power efficient DisplayPort (7.0). In the final stage, the power efficient design of DisplayPort (7.0) is implemented on UtlraScale FPGA. In the next, the each design stage is discussed in detail.

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A. Design Stage 1: vhdl based DisplayPort (7.0)

The DisplayPort (7.0) is designed in Xilinx Vivado Suite using vhdl. The elaborated/schematic design of DisplayPort (7.0) is shown in Figure 2.

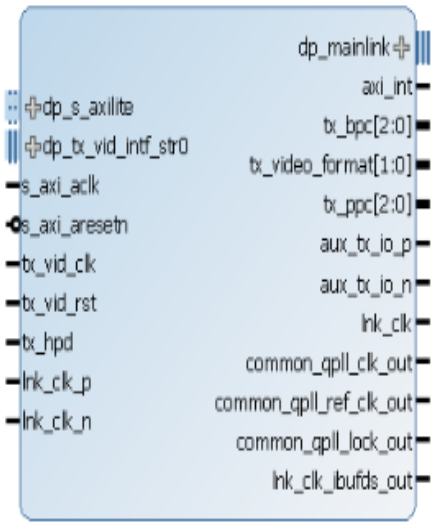

Figure 2. Schematic design of vhdl based DisplayPort (7.0)

The vhdl based design of DisplayPort (7.0) is configured using different parameters these parameters includes; number of lane =1, maximum link speed is 5.6 Gb/s, the clock frequency is 40 GHz, IO location internal, the bit size of frame is 16 bit, maximum bits per color is 16 with dual pixel enable mode. There are different clock signal are included in vhdl based design of DisplayPort (7.0) in order to synchronize the transmitter and receiver. The vhdl based design of DisplayPort (7.0) is also configured with video and audio pins. In this work, the audio pin is disabled. In the next, the vhdl based design of DisplayPort (7.0) is internally configured for the Io Standard design.

B. Design Step 2: IO Standard based HDMI based Video PHY controller

In UltraScale FPGA an I/O tile is defined with I/O buffers, I/O logics and I/O delays. Each IOB contains both input and output logic and IO drivers. These drivers can be configured to various I/O standards [11]. The IO Standard based vhdl based design of DisplayPort (7.0) is configured using Internal AUX IO configuration. This option is bult-in vivado suite to enable or disable the IO Standard for vhdl based design of DisplayPort (7.0). For this reason, the schematic diagram is not shown for IO Standard based vhdl based design of DisplayPort (7.0). This is very important to note that the power analysis for IO Standard based vhdl based design of DisplayPort (7.0) is recorded using same IO Standard internal enable and disable check option. Firstly, vhdl based design of DisplayPort (7.0) power analysis is performed at different high frequencies by disabling the IO Standard option. After that vhdl based design of DisplayPort (7.0) power analysis is performed at different high frequencies by enabling the IO Standard option. Finally, the power consumption is compared for vhdl based design of DisplayPort (7.0) and IO Standard based vhdl based design of DisplayPort (7.0). Virtex UltraScale FPGA support many IO Standard a long list is available in [11]. In this research, authors have selected the LVDS IO Standards, the reason for selecting the LVDS IO Standard is that LVDS offers the electrical characteristics of the serial communications protocol with differential characteristics. LVDS functions at low power and offers high-speed

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interface for high speed application. Due to this LVDS IO Standard is most obvious choice for the vhdl based design of DisplayPort (7.0). In the next, the LVDS IO Standard is configured for vhdl based design of DisplayPort (7.0).

1) Low-voltage differential signaling (LVDS) IO Standard

Low-voltage differential signaling (LVDS) is a powerful high-speed interface IO Standard for different applications. The LVDS IO Standard requires a 1.8 operating voltage. The LVDS is configured with another IO standard that is LVDS_ 25 IO Standard that has the operating voltage of 2.5 V. L. The syntax for changing the IO Standards from default to user defined IO Standards (LVDS/ LVDS_25) is:

a)

```
attribute IOSTANDARD : string;
attribute IOSTANDARD of IDIOA0 : label is- "LVDS";
```

b)

```
attribute IOSTANDARD : string;
attribute IOSTANDARD of IDIOA0 : label is- "LVDS_25";
```

In the next, the power analysis for IO Standard based vhdl based design of DisplayPort (7.0) is observed for using IO Standard and without using IO Standard at different high frequencies.

C. Design Stage 3: Power Analysis of vhdl based design of DisplayPort (7.0) uisng Without IO Standard and With IO Standard

The power analysis of vhdl based design of DisplayPort (7.0) is analyzed for high frequencies 500 MHz, 700 MHz, 1 GHz, and maximum frequency of 1.65 GHz. The power analysis for vhdl based design of DisplayPort (7.0) in UltraScale FPGA power is comprises of sum of device static power, design static power and design dynamic power presented in equation (1) [9].

$$Total\ FPGA\ power = Design\ Dynamic\ Power + Device\ Static\ Power + Design\ Static\ Power \quad (1)$$

Device static power characterizes the transistor leakage power when devices is powered and not configured. Design Dynamic power epitomizes the power associated with design activity and switching events in the core or I/O of the device. Dynamic power is determined by node capacitance, supply voltage, and switching frequency. Design static power denotes the power consumption when the device is configured with no switching activates. The power consume by clock manager. The total on-chip power is measured for different frequencies 500 MHz, 700 MHz, 1 GHz, and 1.65 GHz for vhdl based design of DisplayPort (7.0) without using the IO Standard and using the LVDS IO Standard for maximum lane rate of 5.4 Gb/s.

1) Power Analysis of vhdl based design of DisplayPort (7.0) uisng Without IO Standard

The total on-chip power is measured for different frequencies 500 MHz, 700 MHz, 1 GHz, and 1.65 GHz for vhdl based design of DisplayPort (7.0) without using the IO Standard. The total on-chip power is consisted of Design Dynamic Power + Device Static Power + Design Static Power. The power consumption for vhdl based design of DisplayPort (7.0) without using the IO Standard at 500 MHz is illustrated in Table 1.

Table 1. Power Consumption in W of vhdl based design of DisplayPort (7.0) without using the IO Standard at 500 MHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
25	0.001	5	30.001

It is illustrated in Table 1 that when vhdl based design of DisplayPort (7.0) is operated at 500 MHz without using the IO Standard. The total on-chip power consumption is 30.001W. In this, the maximum power consumption is 25 W for design dynamic power without IO Standard and after that 5 W is for design static power consumption and 0.001 W for device static power in standby mode. The power consumption for vhdl based design of DisplayPort (7.0) without using the IO Standard at 700 MHz is noted in Table 2.

Table 2. Power Consumption in W of vhdl based design of DisplayPort (7.0) without using the IO Standard at 700 MHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
28.2	0.0015	5.8	34.0015

Table 2 shows the on-chip power consumption for vhdl based design of DisplayPort (7.0) operated at 700 MHz without using the IO Standard. The total on-chip power consumption is 34.0015 W. It can be analyzed that when operating frequency is increased the power consumption is also increased. Similarly, the power consumption for vhdl based design of DisplayPort (7.0) without using the IO Standard at 1 GHz is shown in Table 3.

Table 3. Power Consumption in Wof vhdl based design of DisplayPort (7.0) without using the IO Standard at 1.0 GHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
38.2	0.0029	6.7	44.9029

It is clarified in Table 3 that when vhdl based design of DisplayPort (7.0) is operated at 1 GHz without using the IO Standard. The total on-chip power consumption is 44.9029 W. In this, the maximum power consumption is 38.2 W for design dynamic power without IO Standard and after that 6.7 W is for design static power consumption and 0.001 W for device static power in standby mode. The power consumption for vhdl based design of DisplayPort (7.0) without using the IO Standard at 1.6 GHz is noted in Table 4.

Table 4. Power Consumption in W of vhdl based design of DisplayPort (7.0) without using the IO Standard at 1.6 GHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
48.6	0.0056	7.2	55.8056

Table 4 displays the on-chip power consumption for vhdl based design of DisplayPort (7.0) operated at 1.6 GHz without using the IO Standard. The total on-chip power consumption is

55.8056 W. It can be analyzed that when operating frequency is increased the power consumption is also increased.

2) Power Analysis of vhdl based design of DisplayPort (7.0) uisng LVDS_25 IO Standard

The total on-chip power is measured for different frequencies 500 MHz, 700 MHz, 1 GHz, and 1.65 GHz for vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard. The power consumption for vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard at 500 MHz is explained in Table 5.

Table 5. Power Consumption in W of vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard at 500 MHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
5	0.000	0.1	5.1

Table 5 defines the power consumption of vhdl based design of DisplayPort (7.0) operated at 500 MHz using the LVDS_25 IO Standard. The total on-chip power consumption is 5.1 W. The power consumption of vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard is reduced compared to vhdl based design of DisplayPort (7.0) without using IO Standard. It is also important to note that device static power is 0. It means no more consumption recorded in standby mode. Similarly, the power consumption for vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard at 700 MHz is noted in Table 6.

Table 6. Power Consumption in W of vhdl based design of DisplayPort (7.0) using the LVDS_25 IO Standard at 700 MHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
8	0.0	1.7	8.7

It is illustrated in Table 6 that on-chip power consumption for vhdl based design of DisplayPort (7.0) operated at 700 MHz using LVDS_25 IO Standard is 8.7 W. It is demonstrated that power consumption for 700 MHz for vhdl based design of DisplayPort (7.0) using LVDS_25 is less compared to vhdl based design of DisplayPort (7.0) using without IO Standard. The power consumption of vhdl based design of DisplayPort (7.0) using LVDS_25 for 1 GHz is shown in Table 7.

Table 7. Power Consumption in W of vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard at 1.0 GHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
10.2	0.000	2.3	10.5

It is explained in Table 7 that when vhdl based design of DisplayPort (7.0) is operated at 1 GHz using LVDS_25 IO Standard. The total on-chip power consumption is 10.5 W, with device static power of 0.0 W. The power consumption for vhdl based design of DisplayPort (7.0) using LVDS_ 25 IO Standard at 1.6 GHz is noted in Table 8.

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Table 8. Power Consumption in W of vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard at 1.6 GHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
12.3	0.001	2.9	15.201

Table 8 displays the on-chip power consumption for vhdl based design of DisplayPort (7.0) operated at 1.6 GHz using LVDS_25 IO Standard. The total on-chip power consumption is 15.201 W. It can be analyzed that for 1.6 GHz, which is the maximum frequency of vhdl based design of DisplayPort (7.0), the device static power is 0.001 W. It means some of the power consumption is recorded in standby mode.

3) Power Analysis of vhdl based design of DisplayPort (7.0) uisng LVDS O Standard

The power analysis for vhdl based design of DisplayPort (7.0) using LVDS Io Standard is analyzed for 500 MHz, 700 MHz, 1 GHz, and 1.65 GHz. The power consumption for vhdl based design of DisplayPort (7.0) using LVDS IO Standard at 500 MHz is explained in Table 9. Table 9 shows the power consumption of vhdl based design of DisplayPort (7.0) operated at 500 MHz using the LVDS IO Standard. The total on-chip power consumption is 2.19 W.

Table 9. Power Consumption in W of vhdl based design of DisplayPort (7.0) using LVDS IO Standard at 500 MHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
2.1	0.000	0.09	2.19

It is determined that 92% power consumption is reduced for vhdl based design of DisplayPort (7.0) using the LVDS IO Standard compared to vhdl based design of DisplayPort (7.0) without using IO Standard. It is also recorded 52 % power consumption is reduced for vhdl based design of DisplayPort (7.0) using LVDS IO Standard compared to vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard. It is also determined that device static power is recorded for vhdl based design of DisplayPort (7.0) using LVDS IO Standard is 0.0 W. The on-chip power consumption for vhdl based design of DisplayPort (7.0) for without using IO Standard, using LVDS_25 IO Standard and using LVDS IO Standard at 500 MHz is shown in Figure 3.

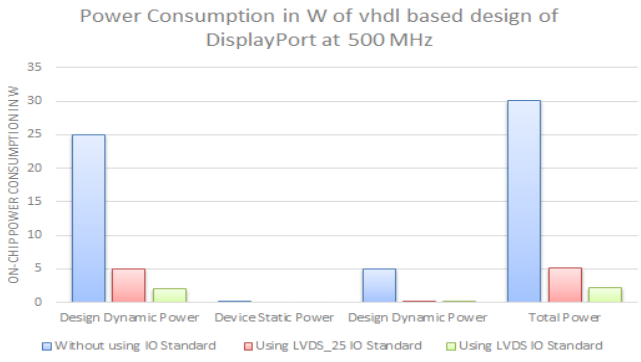

Figure 3. On-chip power consumption for vhdl based DisplayPort (7.0) at 500 MHz

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Similarly, the power consumption for vhdl based design of DisplayPort (7.0) using LVDS IO Standard for 700 MHz is illustrated in Table 10. It is shown in Table 10 that total on-chip power consumption is 3.01 W, the no standby power consumption.

Table 10. Power Consumption in W of vhdl based design of DisplayPort (7.0) using the LVDS IO Standard at 700 MHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
2.9	0.000	0.11	3.01

It is calculated that 65% power consumption is reduced for vhdl based design of DisplayPort (7.0) using LVDS IO Standard compared to vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard. It is also determined that 92% power consumption is reduced for vhdl based design of DisplayPort (7.0) using the LVDS IO Standard compared to vhdl based design of DisplayPort (7.0) without using IO Standard. The on-chip power consumption for vhdl based design of DisplayPort (7.0) for without using IO Standard, using LVDS_25 IO Standard and using LVDS IO Standard at 500 MHz is shown in Figure 4.

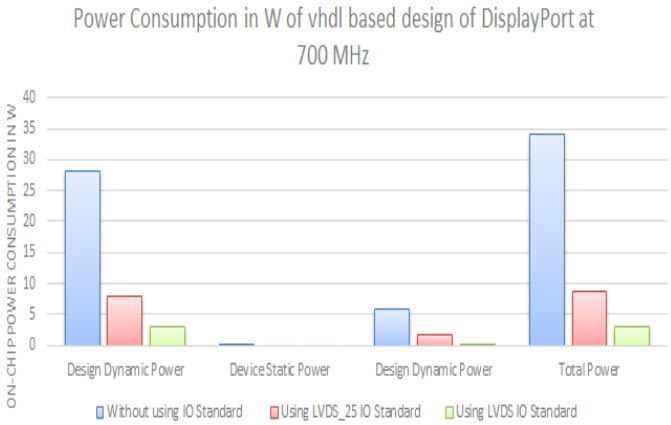

Figure 4. On-chip power consumption for vhdl based DisplayPort (7.0) at 700 MHz

The power consumption of vhdl based design of DisplayPort (7.0) using LVDS IO Standard at 1 GHz is measured in Table 11. It is described in Table 11 that total on-chip power consumption for vhdl based design of DisplayPort (7.0) is 3.47 W, the no power consumption in standby mode.

Table 11. Power Consumption in W of vhdl based design of DisplayPort (7.0) using LVDS IO Standard at 1.0 GHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
3.65	0.000	0.23	3.88

It is shown in Table 11 that 92% power consumption is reduced for vhdl based design of DisplayPort (7.0) using the LVDS IO Standard compared to vhdl based design of DisplayPort (7.0) without using IO Standard. It is also recorded 63% power consumption is reduced for vhdl based design of DisplayPort (7.0) using LVDS IO Standard compared to vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard. The on-chip power consumption for vhdl based design of DisplayPort (7.0) for without using IO Standard, using LVDS_25 IO Standard and using LVDS IO Standard at 500 MHz is shown in Figure 5.

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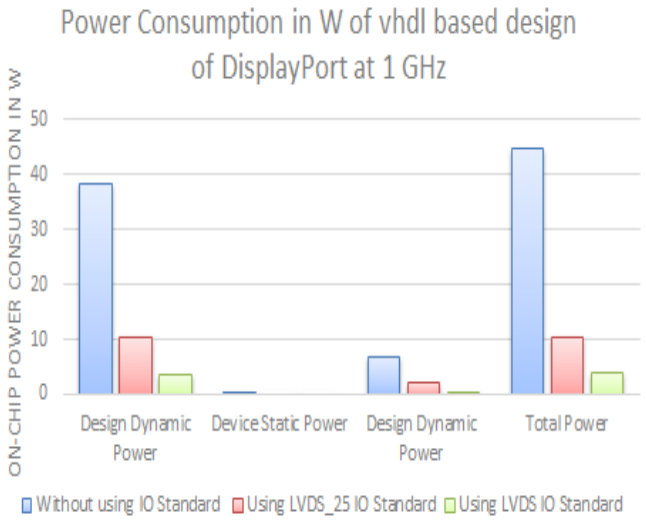

Figure 5. On-chip power consumption for vhdl based DisplayPort (7.0) at 1.0 GHz

Table 12 displays the on-chip power consumption for vhdl based design of DisplayPort (7.0) operated at 1.6 GHz using LVDS IO Standard. The total on-chip power consumption is 4.13 W.

Table 12. Power Consumption in W of vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard at 1.6 GHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
3.82	0.000	0.31	4.13

It is premeditated that 72% power consumption is reduced for vhdl based design of DisplayPort (7.0) using LVDS IO Standard compared to vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard. It is also determined that 93% power consumption is reduced for vhdl based design of DisplayPort (7.0) using the LVDS IO Standard compared to vhdl based design of DisplayPort (7.0) without using IO Standard. It is also important to note that device static power is 0.0 for the high frequency of 1.6 GHz operation of vhdl based design of DisplayPort (7.0). The on-chip power consumption for vhdl based design of DisplayPort (7.0) for without using IO Standard, using LVDS_25 IO Standard and using LVDS IO Standard at 500 MHz is shown in Figure 6.

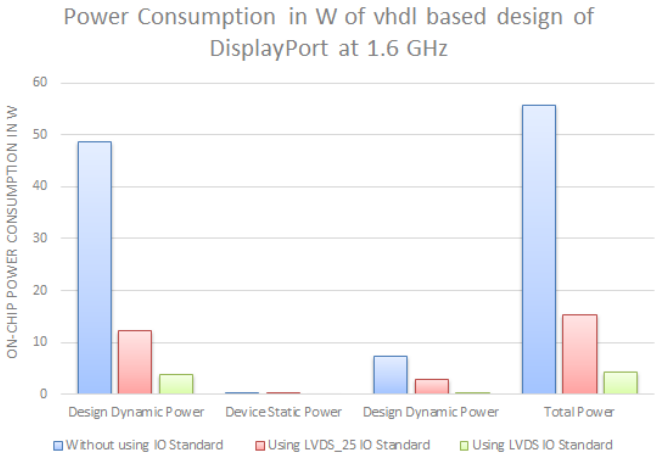

Figure 6. On-chip power consumption for vhdl based DisplayPort (7.0) at 1.6 GHz

In this section, the power analysis for vhdl based design of DisplayPort (7.0) is discussed for without using IO Standard, using LVDS_25 IO Standard, and using LVDS IO Standard. In the next, the results are discussed for proposed power efficient design for vhdl based design of DisplayPort (7.0).

III. RESULTS AND DISCUSSION

In this paper, power efficient design vhdl based design of DisplayPort (7.0) is proposed using LVDS IO Standard. The IO Standard are selected according to specification of vhdl based design of DisplayPort (7.0) and UltraScale FPGA. It is determined that for vhdl based design of DisplayPort (7.0) is tested for 500 MHz, 700 MHz, 1 GHz, and 1.6 GHz using without IO Standard, using LVDS_25 IO Standard and LVDS IO Standard. The power analysis for vhdl based design of DisplayPort (7.0) using proposed technique operated at different frequencies of 500 MHz, 700 MHz, 1.0 GHz, and 1.6 GHz are demonstrated using Figure 7. It is shown in Figure 7 that total on-chip power is calculated for vhdl based design of DisplayPort (7.0) for 500 MHz, 700 MHz, 1.0 GHz, and 1.6 GHz using without IO Standard technique, using LVDS_25 IO Standard technique, and using LVDS IO Standard technique.

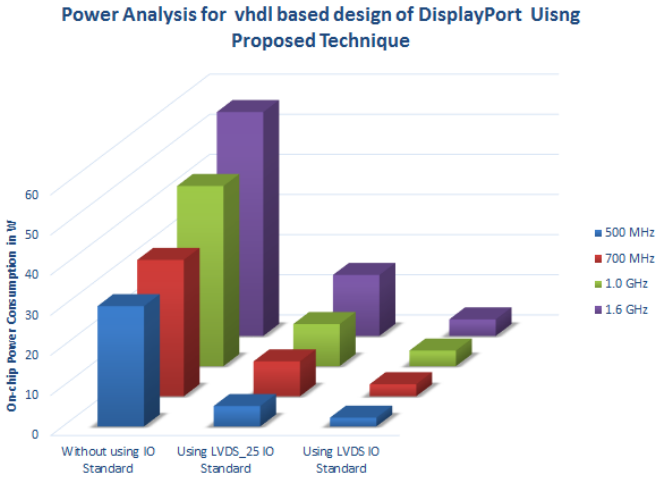

Figure 7. Power analysis for vhdl based DisplayPort (7.0) using proposed technique

It can analyzed from Figure 7 that when vhdl based design of DisplayPort (7.0) without using IO Standard is operated at 500 MHz, 700 MHz, 1.0 GHz, and 1.6 GHz, the maximum power consumption is recorded. When, the vhdl based design of DisplayPort (7.0) is designed using LVDS IO Standard for all frequencies power reduction is achieved compared to vhdl based design of DisplayPort (7.0) without using IO Standard. It can be observed from Figure 7 that when vhdl based design of DisplayPort (7.0) is designed using LVDS IO Standard, minimum power consumption is recorded compared to bath vhdl based design of DisplayPort (7.0) is designed using LVDS IO Standard and vhdl based design of DisplayPort (7.0) without using IO Standard. It is determined vhdl based design of DisplayPort (7.0) operated at 500 MHz using LVDS IO Standard 92% power reduction is attained compared to vhdl based design of DisplayPort (7.0) without using IO Standard and 52% power reduction is achieved consumption is reduced for vhdl based design of DisplayPort (7.0) using LVDS IO Standard compared to vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard. For operating frequency of 700 MHz, when vhdl based design of DisplayPort (7.0) is designed using LVDS IO Standard 65% and 92% power reduction is recorded compared to vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard and vhdl based design of

DisplayPort (7.0) without using IO Standard respectively. It has been observed that for 1.0 GHz, the power reduction of 92% and 63% is attained for vhdl based design of DisplayPort (7.0) using LVDS IO Standard compared to vhdl based design of DisplayPort (7.0) without using IO Standard and vhdl based design of DisplayPort (7.0) using LVDS_25 IO Standard respectively. Finally, 72% and 93% power reduction is achieved for vhdl based design of DisplayPort (7.0) using the LVDS IO Standard compared to vhdl based design of DisplayPort (7.0) using LVDS_25IO Standard and vhdl based design of DisplayPort (7.0) using without IO Standard. It is also determined that device static power is recorded for vhdl based design of DisplayPort (7.0) using LVDS IO Standard is 0.0 W. It means for all frequencies; 500 MHz, 700 MHz, 1.0 GHz, and 1.6 GHz, the standby power consumption is none. The vhdl based design of DisplayPort (7.0) using LVDS IO Standard will be helpful to produce high resolution video at low power consumption. In the future, the power efficient design of vhdl based design of DisplayPort (7.0) using LVDS IO will consume less power for high resolution video.

IV. ACKNOWLEDGEMENT

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