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Frequency Scaled Green Data Flip Flop on Different Nanometer Technology Based FPGA

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Abstract

In order to meet the energy requirement of the total population of the globe, we have designed an energy efficient data flip flop on different nanometer technology-based FPGA. We used frequency scaling technique in order to analyze power dissipation. The power has been analyzing for Virtex 6 (40nm) FPGA, Spartan 3 (90nm) FPGA, Spartan 6 (45nm FPGA). We varied the frequency from 10 MHz to 100 GHz and observed the different powers of chips which are clustered on data flip flop, e.g. Clocks, Signals, I/O, Leakage, and Total power. We observed that at low frequency, there is less power dissipation whereas at high frequency more power is dissipated.

Keywords: *Spartan 6, Spartan 3, Virtex 6, FPGA, Power, Frequency*

I. INTRODUCTION

Now a day's energy requirements for the total population of the globe is very difficult [1]. In order to fulfil the requirement of green communication we are making an energy efficient data flip flop. Flip flops are one of the major devices in communication. We all know that these devices are used in storing data in a communication network. But storing the data with minimum power dissipation will be a major step towards green communication. So, for frequency scaling technique we are analyzing the power dissipation of data flip flop on different nanometer technology-based FPGA. As clock frequency is reduced less time is required by data to reach at input. And at low value of frequency there is minimum power dissipation. The schematic of data flip flop implemented on Xilinx 14.1 ISE Design is shown in Fig. 1.

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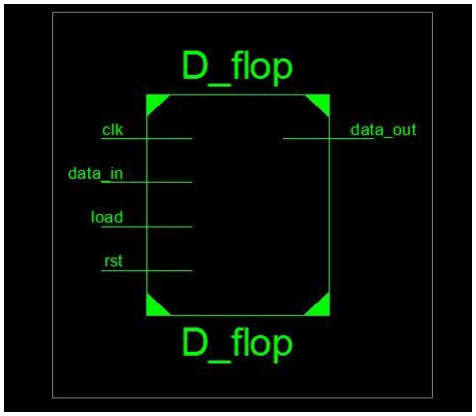

Fig. 1. Schematic of D Flip Flop.

Fig. 2 and Fig. 3 respectively shows the RTL and Technology schematic of data flip flop as frequency increases power dissipation also increases and at 100 GHz frequency, Spartan 3 FPGA stops working.

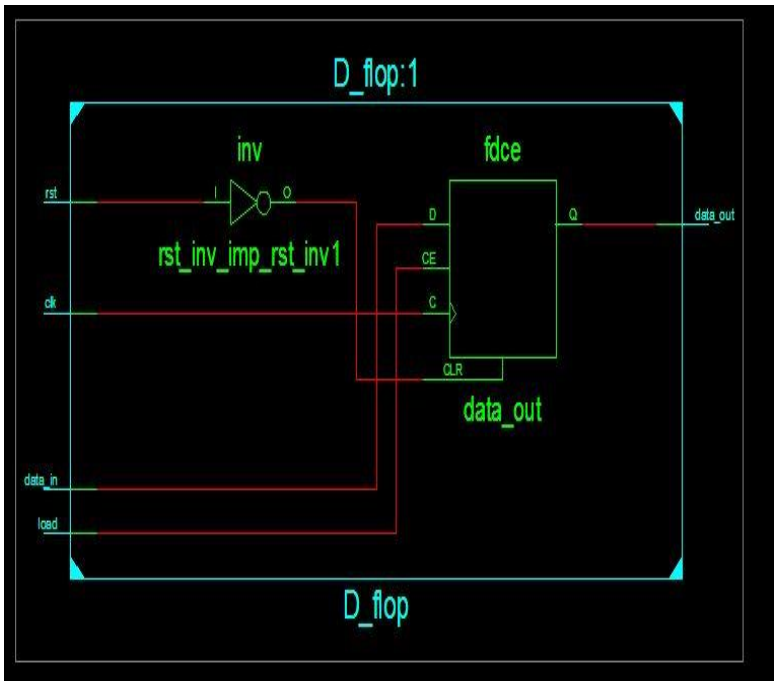

Fig. 2. RTL Schematic of D Flip Flop.

II. Related Work

D. Jones et. al [2] presented an architecture for FPGA towards logic emulation to achieve maximum usable logic density per unit silicon area and test mapping. S. Trimberger et. al [3] proposed the architecture of a time multiplexed FPGA. In [4] authors analyzed the dynamic power consumption in fabric of FPGA using Virtex-II family. In this power of routing, logic, clock power dissipation is measured. W. Zhao et.al [5] proposed a low power dissipation and high-speed nonvolatile flip flop. This work was based on magnetic ram technology on standard CMOS. Singh [6] used voltage and frequency

scaling technology to design an energy efficient flip flop design on FPGA. F. Serrano [7] presented an idea to emulate single event upset in FPGA and flip flops. But in our work, we are designing an energy efficient data flip flop to full fill the requirement of green communication.

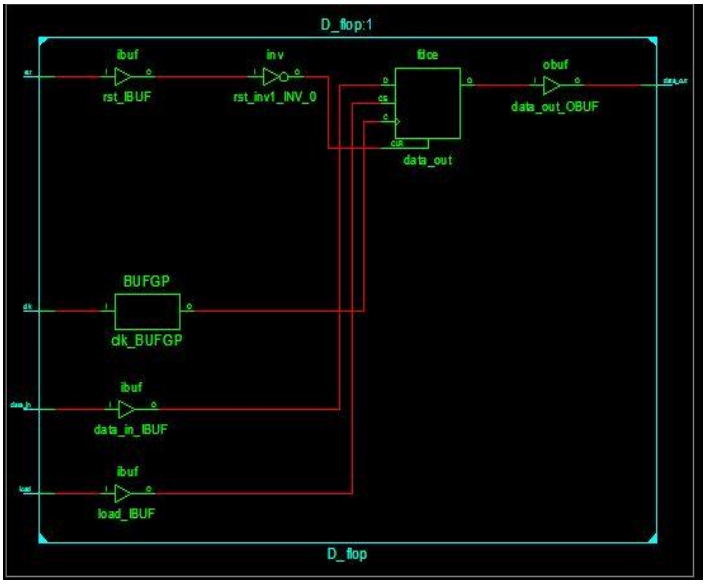

Fig. 3 Technology Schematic of D Flip Flop.

III. Experimental Section

Our experiment was implemented on Xilinx 14.1 ISE Design simulator using Virtex-6, Spartan 3 and Spartan 6 FPGA family. The frequency of flip flop is varied from 10MHz to 100GHz. XPower Analyzer tool is used to calculate the power.

IV. Power Analysis

A. Power Analysis at 10 MHz Frequency

At 10 MHz, we observed that Spartan 6 FPGA dissipates least amount of clock, signal, I/O, leakage and total power. The power table of Spartan 6, Spartan 3 and Virtex 6 FPGA is shown in Table 1. And in Fig. 4, comparison of power dissipation of Spartan 6, Spartan 3 and Virtex 6 has shown.

Table 1. Power analysis of Spartan 6, Spartan 3 and Virtex 6 FPGA.

Power on chip(W)	Spartan -6	Spartan -3	Virtex-6
Clock	0.001	0.000	0.000
Signal	0.000	0.000	0.000
I/O	0.000	0.000	0.000
Leakage	0.014	0.027	1.293
Total	0.014	0.028	1.293

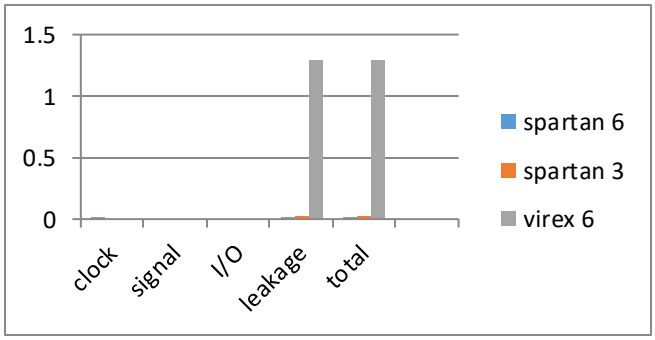

Fig. 4. Power Comparison of Spartan 6, Spartan 3, Virtex 6.

B. Power Analysis at 100 MHz Frequency

Power table at 100 MHz frequency is shown in Table 2. At this value of frequency Spartan 6 consumes least amount of Clock, Signal, I/O, Leakage and Total Power from the other two FPGA used. Power comparison figure is shown in Fig. 5.

Table 2. Power Analysis of Spartan 6, Spartan 3 and Virtex 6 FPGA.

Power on chip(W)	Spartan -6	Spartan -3	Virtex-6
Clock	0.002	0.001	0.003
Signal	0.000	0.000	0.000
I/O	0.000	0.004	0.000
Leakage	0.014	0.027	1.293
Total	0.015	0.033	1.296

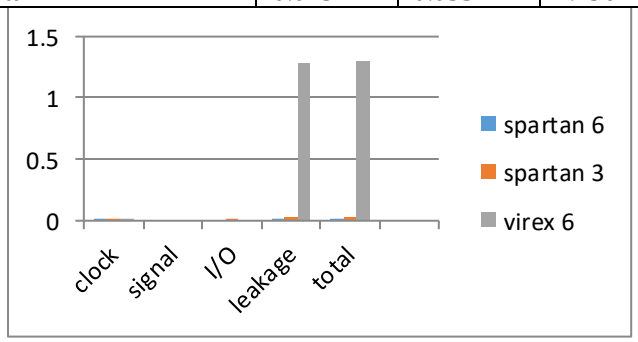

Fig. 5. Power Comparison of Spartan 6, Spartan 3, Virtex 6.

C. Power Analysis at 1 GHz Frequency

At 1 GHZ frequency when the power consumption of three FPGA are compared it is observed that Spartan 6 consumes least amount of power whereas Virtex 6 uses the maximum power. The power table and the power comparison figure are shown in Table 3 and Fig. 6 respectively.

Table 3. Power analysis of Spartan 6, Spartan 3 and Virtex 6 FPGA

Power on chip(W)	Spartan -6	Spartan -3	Virtex-6
Clock	0.011	0.014	0.030
Signal	0.000	0.000	0.001
I/O	0.002	0.014	0.004

Leakage	0.014	0.028	1.294
Total	0.027	0.086	1.329

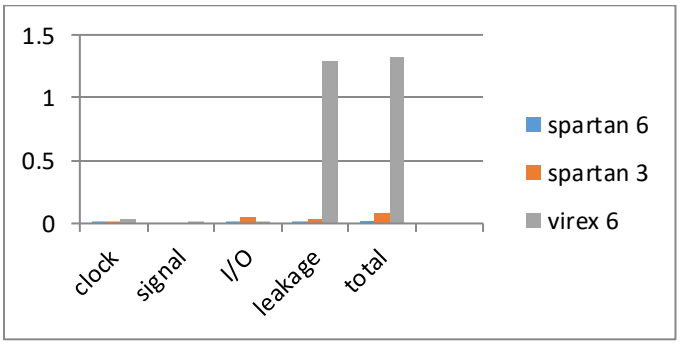

Fig. 6. Power Comparison of Spartan 6, Spartan 3, Virtex 6.

D. Power Analysis at 10 GHz Frequency.

The power table at 10 GHz frequency is shown in table 4. And power comparison has shown in Fig. 7.

Table 4. Power analysis of Spartan 6, Spartan 3 and Virtex 6 FPGA

Power on chip*(W)*	Spartan-6	Spartan-3	Virtex-6
Clock	0.111	0.142	0.305
Signal	0.001	0.001	0.000
I/O	0.015	0.439	0.056
Leakage	0.015	0.030	1.301
Total	0.141	0.611	1.668

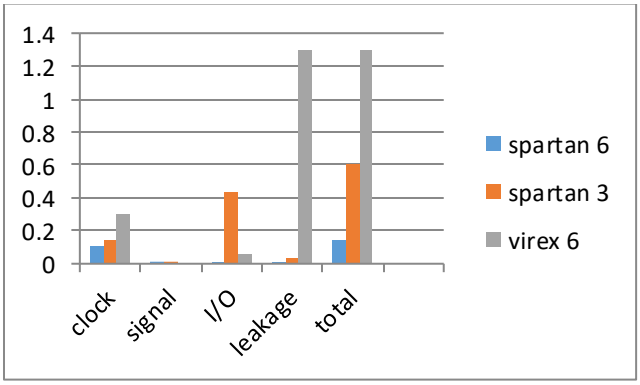

Fig. 7. Power Comparison of Spartan 6, Spartan 3, Virtex 6.

E. Power Analysis at 100 GHz Frequency

At such a high frequency of 100 GHz Spartan 3 stops working and the power dissipation is least in Spartan 6 FPGA. The power table and power comparison figure is shown in Table 5 and Fig. 8 respectively.

Table 5. Power analysis of Spartan 6, Spartan 3 and Virtex 6 FPGA

Power on chip *(W)*	Spartan-6	Spartan-3	Virtex-6
Clock	1.101	1.416	3.049
Signal	0.006	0.008	0.063
I/O	0.153	0.002	0.560
Leakage	0.040	4.381	1.380
Total	1.300	10.036	5.053

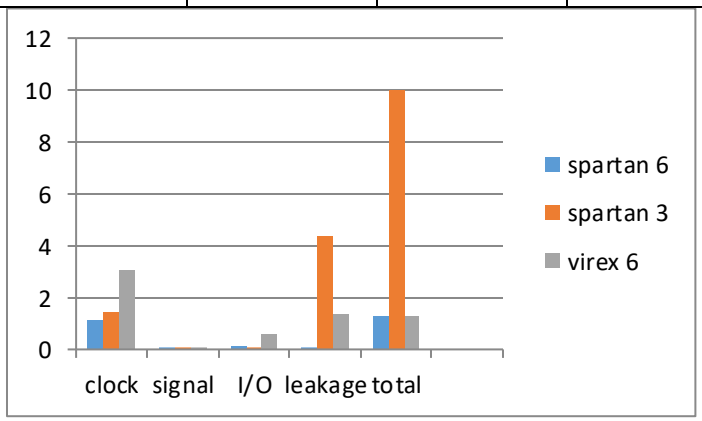

Fig. 8. Power Comparison of Spartan 6, Spartan 3, Virtex 6.

V. Results

In this through experiment it is observed that Spartan 6 is the most power efficient FPGA. When compared with Spartan 3 and Virtex 6 at 10 MHz frequency, Spartan 6 consumes 48.14% less leakage power than Spartan 3 and 98.917% less leakage power than Virtex 6. In case of total power Spartan 6 consumes 50% less power than Spartan 3 and 98.917% less power than Virtex 6. When the three FPGA are compared at 100 MHz frequency, we found that Spartan 3 consumes least amount of clock power but the leakage and the total power is consumed less by Spartan 6 and maximum by Virtex 6. For clock power the percentage deviation of Spartan 3 is 50% less from Spartan 6 and 66.66% less from Virtex 6. For leakage power Spartan uses 48.148% less power than Spartan 3 and 98.917% less power than Virtex 6. And for total power Spartan 6 FPGA uses 54.545% less power than Spartan 3 and 98.842% less than Virtex 6.When the frequency is 1 GHz it is found that Spartan 6 consumes the least of all Clock, Signal, I/O, Leakage and Total Power, it is 21.428% less than Spartan 3 and 63.33% less than Virtex 6 for clock power. For I/O Spartan 6 uses 85.714% less than Spartan 3 and 50% less than Virtex 6. For leakage and total power, it is 50% less than Spartan 3 and 98.918% less than Virtex 6 and 68.604%less than Spartan 3 and 97.968% less than Virtex 6 respectively. For 10 GHZ frequency also Spartan 6 is most power efficient. The change in percentage of power less than Spartan 3 for Clock, I/O, Leakage and Total Power is given as 21.83%, 96.583%, 50%, and 76.92% respectively. The percentage of Clock, I/O, Leakage and total power is used by Spartan 6 when compared with Virtex 6 is as 63.606%,73.214%,98.897%,91.526% respectively. When the frequency reaches 100 GHz, we found that Spartan 6 stops working, Spartan 6 consumes the least amount of power than Virtex 6. We found that the percentage change in Clock, Signal, I/O, Leakage and Total Power when compared with Virtex 6 is as follows 63.889%, 90.476%, 72.678%, 97.101%, 74.272% respectively.

VI. Conclusion

Our work represents the power consumption of Virtex-6, Spartan 3 and Spartan 6 FPGA family for energy efficient flip flop design. We did this on Xilinx 14.1 ISE Design simulator. We have scaled the flip flop frequency from 10 MHz to 100GHz and analyzed Clock power, IOs power, leakage power and total power and it was found that Spartan 6 was most power efficient at all frequency value.

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