Gyancity Journal of Electronics and Computer Science,
Vol.4, No.1, pp. 8-13, March 2019
ISSN: 2446-2918 DOI: 10.21058/gjecs.2019.41002

Energy Efficient UART Design Using Virtex-4, Virtex-5 and Virtex-6 FPGA

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Abstract

We analyzed the deviation of various power of chips that are clustered on Universal Asynchronous Receiver Transmitter (UART), for example IOs power, leakage power and total power by varying the voltage supply. We performed our experiment and analyzed how the variation in voltage influences the power of UART chips. We used three different FPGA technology that are Virtex-4, Virtex-5, and Virtex-6 to perform our experiment and analyzed that Virtex-4 is most power efficient.

Keywords: *Virtex-4, Virtex-5, Virtex-6, FPGA, Power, Voltage, UART.*

I. INTRODUCTION

Energy and power deficiency are increasing day by day across the entire globe. The main cause of this energy and power crisis are day by day increasing population and industrialization across the world [1]. That is why it has become very difficult to full fill the demand of energy over entire globe. So to reduce the energy consumption in our day to day life we are designing an UART using Virtex-4, Virtex-5, and Virtex-6 FPGA which requires less amount of power. UART is a communication protocol device [2] which transfers data in both serial and parallel manner. In transfer of data, voltage supply plays an important role in determining the power of UART circuit. We know$P \propto V$ and $P = VI$, therefore we can understand that power is influenced by voltage. Hence if we change the supply voltage the "vccint and thermal properties" changes but all the other parameter of voltage remains same. The voltage parameters which remains same are "VCCAUX, VCCO25, MGTAVcc, MGTAVtt" also there is no effect on thermal resistance to air that is effective TJA as voltage increases.

II. Related Work

In. [4], researcher designed a multichannel UART controller using asynchronous FIFOs (First In First Out) which allows communication with multiple blocks at different baud requirements. In [5], author proposes the addition of BIST techniques to a UART design. In [6], author implements a UART for high speed operations. In [7] authors have developed a tamper resistant design using Virtex-6 & 7 series FPGAs. In [8] authors have optimized the active leakage power using FPGA technology. In [9] using Virtex-5 FPGA authors have designed a power consideration system. In this paper authors have decreased the transistor size, thus leakage current & static power increases.

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III. Experimental Section

We did our experiment on Xilinx 14.1 ISE Design simulator [3] using Virtex-4, Virtex-5, Virtex-6 FPGA family and code of UART is written in Verilog module keeping the frequency of UART at 1GHz. Xpower Analyzer tool is used to calculate the power variation of UART since voltage supply changes from 1.1 V to 1.5 V. The environment in which we implemented our design requires ambient temperature of 50^0C and 250 linear feet per minute (LFM) air flow.

IV. Explanation

The voltage and the corresponding change in IOs, Leakage and Total power of Virtex-4, Virtex-5, and Virtex-6 FPGAs is shown in Table 1, Table 2, and Table 3 respectively.

Table 1. Voltage and Corresponding power of Virtex-4 FPGA.

Voltage Source (Vccint)	IOs Power	Leakage Power	Total Power
1.1 V	0.011 W	0.147 W	0.181 W
1.2 V	0.011 W	0.167 W	0.207 W
1.3 V	0.011 W	0.191 W	0.231 W
1.4 V	0.011 W	0.220 W	0.263 W
1.5 V	0.012 W	0.253 W	0.299 W

Table 2. Voltage and Corresponding power of Virtex-5 FPGA.

Voltage Source (Vccint)	IOs Power	Leakage Power	Total Power
1.1 V	0.014 W	0.439 W	0.470 W
1.2 V	0.014 W	0.613 W	0.646 W
1.3 V	0.015 W	0.869 W	0.904 W
1.4 V	0.015 W	1.250 W	1.287 W
1.5 V	0.015 W	1.822 W	1.861 W

Table 3. Voltage and Corresponding power of Virtex-6 FPGA.

Voltage Source (Vccint)	IOs Power	Leakage Power	Total Power
1.1 V	0.030 W	1.610 W	1.679 W
1.2 V	0.031 W	2.081 W	2.155 W
1.3 V	0.032 W	2.794 W	2.872 W
1.4 V	0.032 W	3.891 W	3.974 W
1.5 V	0.033 W	5.643 W	5.731 W

There is also change in thermal properties of Virtex-4, Virtex-5, and Virtex-6 FPGA when voltage of UART increases. The change is seen in Table 4, Table 5, and Table 6.

Table 4. Thermal properties of Virtex-4 FPGA as voltage increases from 1.1V to 1.5V.

Voltage (V)	Effective TJA (C/W)	Max. Ambient Temp (°C)	Junction Temp. (°C)
1.1	14.7	82.3	52.7
1.2	14.7	82.0	53.0
1.3	14.7	81.6	53.4
1.4	14.7	81.1	53.9
1.5	14.7	80.6	54.4

Table 5. Thermal properties of Virtex-5 FPGA as voltage increases from 1.1V to 1.5V.

Voltage (V)	Effective TJA (C/W)	Max. Ambient Temp (°C)	Junction Temp. (°C)
1.1	2.8	83.7	51.3
1.2	2.8	83.2	51.8
1.3	2.8	82.5	52.5
1.4	2.8	81.4	53.6
1.5	2.8	79.8	55.2

Table 6. Thermal properties of Virtex-6 FPGA as voltage increases from 1.1V to 1.5V.

Voltage (V)	Effective TJA (C/W)	Max. Ambient Temp (°C)	Junction Temp. (°C)
1.1	2.7	80.4	54.6
1.2	2.7	79.1	55.9
1.3	2.7	77.2	57.8
1.4	2.7	74.2	69.4
1.5	2.7	69.4	65.6

IV. POWER ANALYSIS

A. Power analysis of Virtex-4 FPGA.

In Virtex-4 as voltage increases from 1.1V to 1.5V there is almost negligible change in IOs power but leakage and total power varies by a sufficient amount. This variation is seen in Fig. 1.

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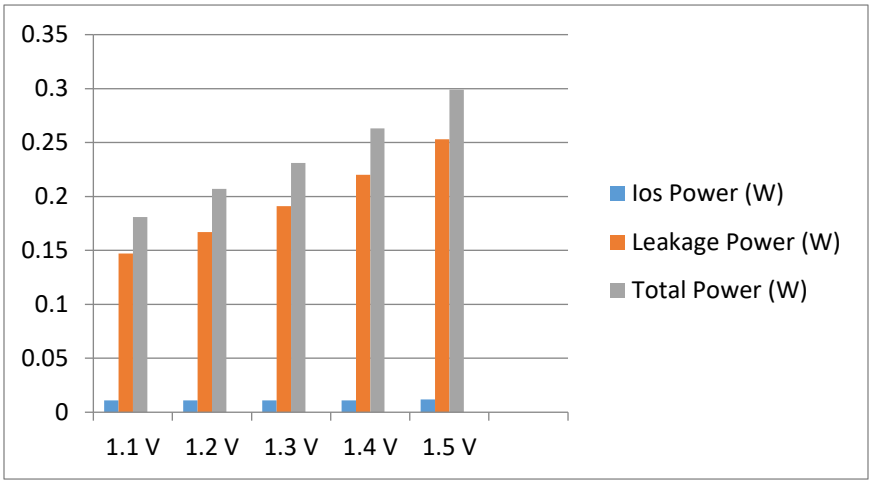

Fig. 1. Power Analysis of Virtex-4 FPGA.

B. Power analysis of Virtex-5 FPGA.

In case of Virtex-5 also there is almost no change in IOs power but leakage and total power changes sufficiently. The power chart is shown in Fig. 2.

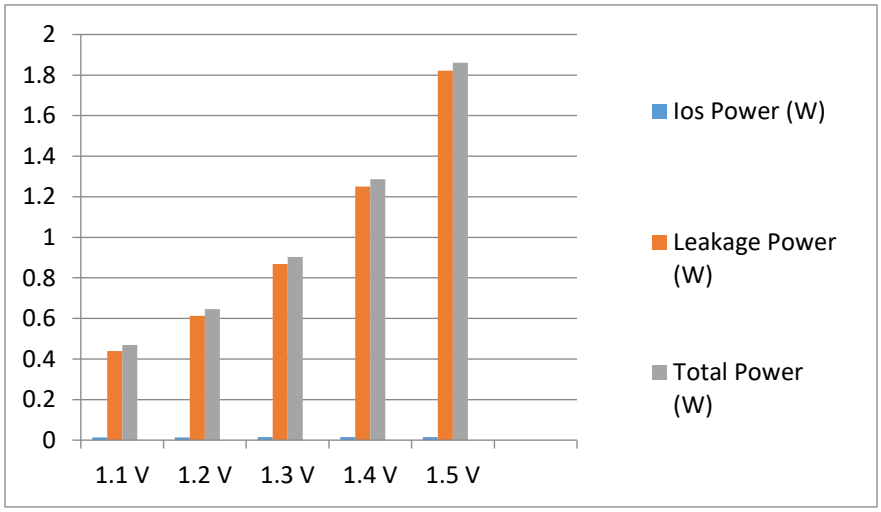

Fig. 2. Power Analysis of Virtex-5 FPGA.

C. Power analysis of Virtex-6 FPGA.

The power analysis of Virtex-6 FPGA follows the same trend as of Virtex-4 and Virtex-5 FPGA. The power analysis is shown in Fig. 3.

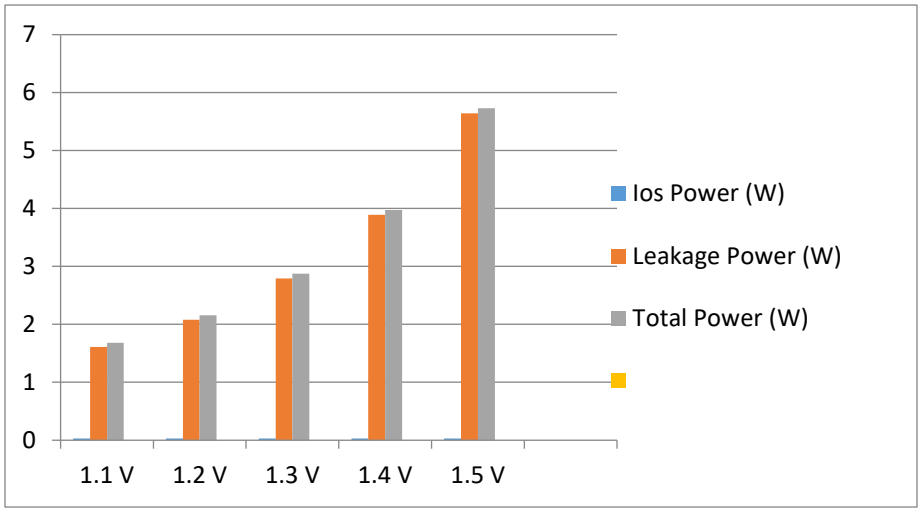

Fig. 3. Power Analysis of Virtex-6 FPGA.

IV. Results

From the experiment it was found that, when voltage was 1.1 *V* Virtex-4 FPGA consumes least amount of IOs, leakage and total power from both Virtex-5 and Virtex-6 FPGA.Virtex-4 consumes 21.42% less IOs power, 66.51% less leakage power and 61.48% less total power than Virtex-5 FPGA. And 63.33% less IOs power, 90.865% less leakage power, and 89.219% less total power than Virtex-6 FPGA. When voltage was 1.5 *V* Virtex-4 is again power efficient. It was 20% and 63.63% less IOs power than Virtex-5 and Virtex-6 FPGA. For leakage power Virtex-4 requires 86.114% less power than Virtex-5 and 95.51% less power than Virtex-6 FPGA. And for total power Virtex-4 uses 83.933 % less power than Virtex-5 and 94.78%% less power than Virtex-6 FPGA.

V. Conclusion

Our work represents the power comparison of Virtex-4, Virtex-5 and Virtex-6 FPGA family for UART design. The frequency at which we did our experiment was 1GHz. We did this on Xilinx 14.1 ISE Design simulator. We have increased UART voltage from 1.1V to 1.5V and analyzed IOs power, leakage power and total power and it was found that Virtex-4 was most power efficient at all voltage value than Virtex-5 and Virtex-6 FPGA family.

REFERENCES

[1] Energy Crisis, en.wikipedia.org/wiki/Energy_crisis, Last Accessed on 28th January 2019

[2] D. Bhadra, V. S. Vij, and K. S. Stevens. "A low power UART design based on asynchronous techniques." In Circuits and Systems (MWSCAS), 2013 IEEE 56th International Midwest Symposium on, pp. 21-24. IEEE, 2013.

[3] A. Kaur, B. Pandey, A. Sharma, K. Sharma, and S. Singh. "SSTL IO Standard Based Tera Hertz and Energy Efficient MALAYALAM Unicode Reader Design and Implementation on FPGA." In DRDO, Ministry of Defence, Government of India: Bilingual International Conference on Information Technology at Defence Scientific Information and Documentation Centre (DESIDOC), pp. 19-21. 2015..

[4] S.Yu, L. Yi, W. Chen, and Z. Wen, “Implementation of a multichannel uart controller based on fifo technique and fpga”, in Industrial Electronics and Application.2007. ICIEA 2007. 2nd IEEE Confrence on, may 2007,pp.2633-2638.

[5] M. Idris and M. Yaacob, “A vhdl implementation of bist technique in uart design,” in TENCON 2003. Conference on Convergent Technologie for the Asia-Pacific Region, vol. 4, Oct., pp. 1450–1454 Vol.4.
[6] J. Norhuzaimin and H. H. Maimun, “The design of high speed uart,” in Applied Electromagnetics, 2005. APACE 2005. Asia-Pacific Conference on, Dec., pp. 5 pp.
[7] Ed. Peterson, "Developing tamper resistant designs with Xilinx Virtex-6 and 7 series FPGAs." Application Note. Xilinx Corporation (2013).
[8] J. H. Anderson, and F. N. Najm. "Active leakage power optimization for FPGAs." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems25, no. 3 (2006): 423-437.
[9] A. Peggy, M. Klein, and B. Philofsky. "Virtex-5 FPGA system power design considerations." Xilinx WP285 (v1. 0) February 14 (2008).