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HSTL and HSUL I/O Standard Based Energy-Efficient Control Unit Circuit Design on FPGA

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Abstract- World is facing a huge problem of power deficiency. That's why power and energy-efficient devices are getting more attention these days. This work highlights the energy-efficient control design implementation on 28nm technology Artix-7 Field Programmable Gate Array (FPGA). The implementation is done on the Vivado 2014.2 Design Suite. In this work, the Input/Output (I/O) Standard is varied at both input and output end of control unit circuit for calculating the power utilization of the control unit circuit with 28-nm FPGA. It is observed that High-Speed Unterminated Logic (HSUL_12) I/O Standard consumes the least amount of power when the control unit circuit is implemented on 28-nm FPGA.

Keywords- Control unit, FPGA, I/O Standard, Energy, and Power.

I. INTRODUCTION

The natural resources of power utilization of each and every country are decreasing day by day. The reduction in power utilization is due to the rapid increase in population and industrialization across the globe [1]. To overcome the problem of energy and power crisis, people are getting more concerned about the technologies of green communication and power-efficient devices [2-3]. This work is a step towards the contribution of green communication technologies. In this work, the control unit circuit is implemented on 28nm Artix-7 FPGA. The control unit is a circuitry component which is attached to the Central Processing Unit (CPU) of a computer [4]. It transfers the data sets to the processor of the CPU. In this work I/O Standard of HSTL and HSUL group is used to calculate the output power of the control unit circuit interfaced with 28nm technology based Artix-7 FPGA.

- ✔ **I/O Standards-** I/O Standards are considered as those logic resources which are used in any electrical circuit for matching the input load, input line, output line, and output load power [5-6].

✔ **HSTL I/O Standards-** It stands for High-Speed Transceiver Logic. This I/O Standard is used for transferring signal in integrated circuits. This I/O Standard works in the voltage range of 0V to 1.5V [7-8]. The different HSTL I/O Standards used in this work are as follows-

- HSTL_I
- HSTL_I_18
- HSTL_II
- HSTL_II_18
- HSUL_12

✔ **HSUL I/O Standards-** It stands for High-Speed Unterminated Logic. This I/O Standard works in the voltage range of 0V to 3.0V [9].

II. RELATED WORK

An energy-efficient Arithmetic Logic Unit (ALU) is designed by authors. Authors used various SSTL I/O standard to calculate the power of device [10]. An energy-efficient Read-Only Memory (ROM) is designed by authors using various SSTL I/O standard techniques [11]. Power efficient and thermal aware adder circuit is designed on 65 nm FPGA using different HSTL I/O standard [12]. Using different nanometer technology-based FPGA, a power-efficient UART is designed by authors [13]. In this research work, Virtex6, 40 nm technology is used and for the coding purpose, Verilog Hardware Description Language (VHDL) is used [14]. High-Performance and low power Vedic multiplier are designed by author's voltage scaling techniques [15]. LVTTL based energy-efficient watermark generator is designed and implemented on FPGA [16]. A power-efficient address register is designed by authors using different nanometer technology-based FPGA [17]. Effect of Different Nano Meter Technology-Based FPGA is observed on UART [18].

III. EXPERIMENTAL AND ENVIRONMENTAL SETUP

The interfacing of the control unit circuit with Artix-7 FPGA is done on Vivado 2014.2 Design Suite. The code of the control unit circuit is coded in one of the famous Hardware description languages called Verilog. The design is implemented at 25^0C and has an airflow of 250 Linear Feet per Minute (LFM). The output load capacitance of the design is kept constant at 5 Pico Farad (Pf) for power calculation. The schematic is presented in figure 1.

IV. INVESTIGATION OF POWER UTILIZATION

Basically, there are two components of power for which power is calculated, which are as follows-

- (i). Static Power – It comprises leakage power of control unit when interfaced with FPGA.
- (ii) Dynamic Power- It includes the Signal power, I/O power, Logic power of control unit when interfaced with FPGA.

A. Investigation of Power Utilization with usage of HSTL_I I/O Standard.

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When input and output power is matched by using HSTL_I I/O Standard then the total power utilization of the device is 0.404W. The total power utilization is the sum of device static power and dynamic power. Dynamic/Leakage power consumes 76% of the total power which is 0.306 W, while static power takes 24% of the total power which is 0.098W. Static power is the sum of signal power, I/O power and, logic power which are 0.026W, 0.264W and, 0.016W respectively. In figure 2 power utilization of HSTL_I I/O Standard interfaced with the control unit circuit on Artix-7 FPGA is described.

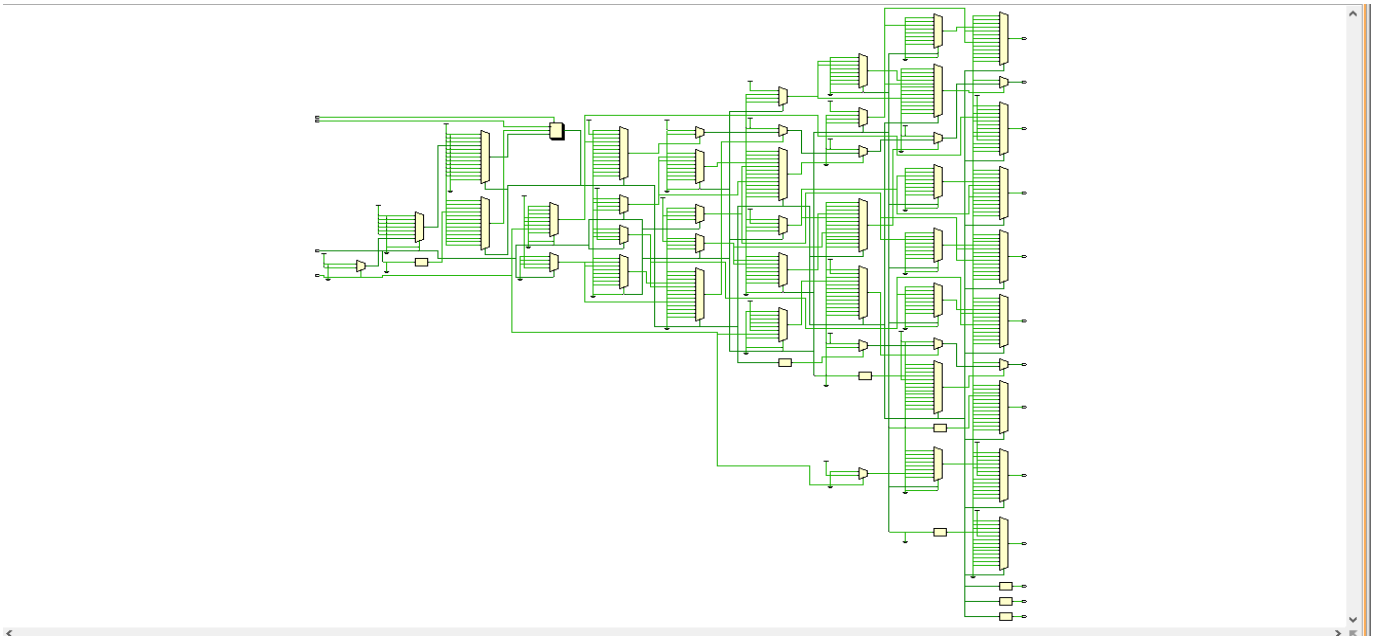

Figure 1. RTL Schematic of Control Unit.

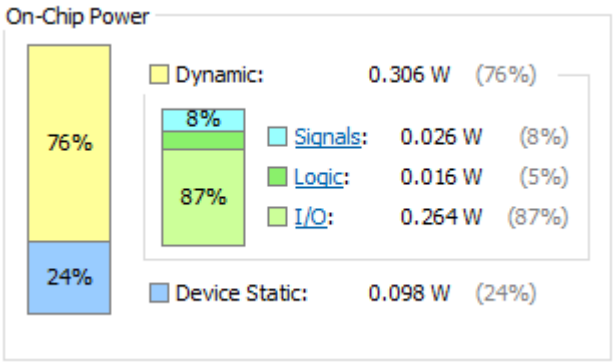

Figure 2. Power utilization of control unit with usage of HSTL_I I/O Standard.

B. Investigation of Power Utilization with usage of HSTL_I_18 I/O Standard.

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When HSTL_I_18 I/O Standard is applied for matching the power, it is observed that 77% of the total power is consumed by dynamic/leakage power and only 23% of the total power is consumed by device static power. The total power utilization for HSTL_I_18 I/O Standard is 0.429W which is shown in figure 3.

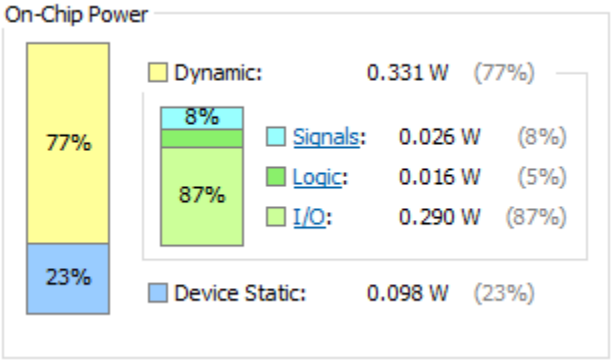

Figure 3. Power utilization of control unit with usage of HSTL_I_18 I/O Standard.

C. Investigation of Power Utilization with usage of HSTL_II I/O Standard.

For HSTL_II I/O Standard, the total power utilization is 0.38W. Leakage/dynamic power consumes 0.282W which is 74% of the total power. Signal, logic and, I/O power consumes 0.026W, 0.016W and, 0.241W respectively. Power utilization of control unit with usage of HSTL_II I/O Standard is shown in figure 4.

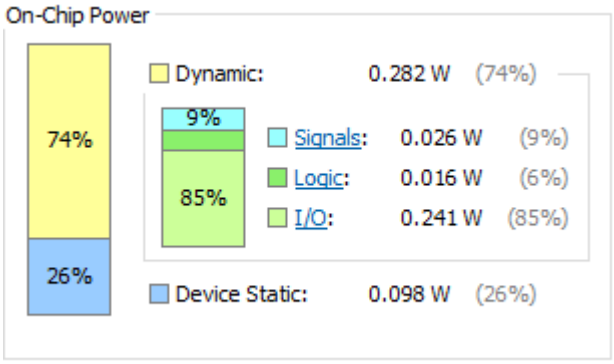

Figure 4. Power utilization of control unit with usage of HSTL_II I/O Standard.

D. Investigation of Power Utilization with usage of HSTL_II_18 I/O Standard.

When HSTL_II_18 I/O Standard is applied for matching the output power, the total power utilization is 0.396W. The total power is the combination of dynamic power and static power of the device which are 0.298W and 0.098W respectively. The total power analysis for HSTL_II_18 I/O standard is shown in figure 5.

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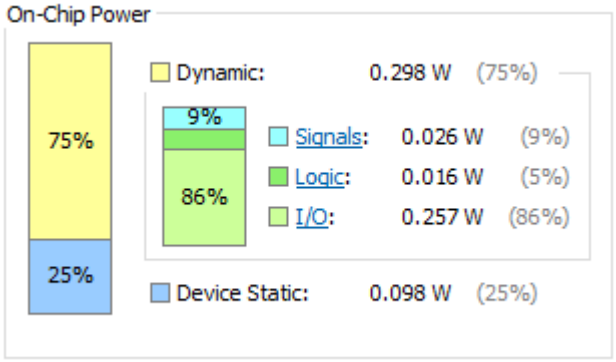

Figure 5. Power utilization of control unit with usage of HSTL_II_18 I/O Standard.

E. Investigation of Power Utilization with usage of HSUL_12 I/O Standard.

When input and output power is matched by using HSUL_12 I/O Standard then the total power utilization of the device is 0.375W. The total power utilization is the sum of device static power and dynamic power. Dynamic/Leakage power consumes 73% of the total power which is 0.273W, while static power takes 27% of the total power which is 0.103W. Static power is the sum of signal power, I/O power and, logic power which are 0.026W, 0.231W and, 0.016W respectively. The power analysis for HSUL_12 I/O Standard is shown in figure 6.

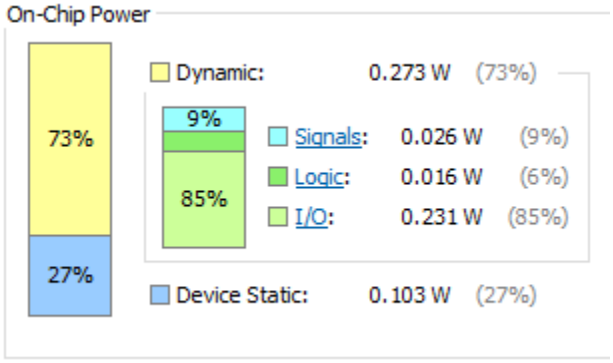

Figure 6. Power utilization of control unit with usage of HSUL_12 I/O Standard.

V. OVERALL POWER UTILIZATION

It is analyzed that HSUL_12 I/O Standard (0.375W) consumes the least amount of power and HSTL_I_18 I/O Standard (0.429W) consumes the highest amount of power. There is an increment of 7.178% of the total power when HSTL_I I/O Standard is compared with HSUL_12 I/O Standard. When the total power of HSTL_I_18 I/O Standard is compared with HSUL_12 I/O Standard, it is observed that the increment of the total power is 12.587%. For the comparison of the total power of HSTL_II and HSTL_II_18 with HSUL_12 I/O Standard, there is an increment of 1.315% and 5.303% respectively. The total power of all the above mentioned I/O standard is shown in figure 7.

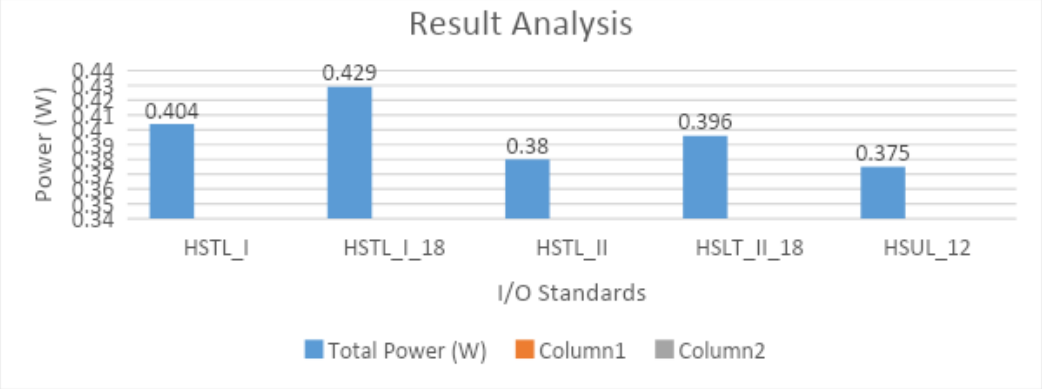

Figure 7. Total Power Analysis.

VI. CONCLUSION

The implementation of the control unit circuit with 28nm Artix-7 FPGA is done on Vivado 2014.2 Design Suite. In this work, the input load and the output load I/O Standard is changed for the power calculation. It is observed that HSUL_12 I/O Standard is most power-efficient I/O Standard. While the HSTL_I_18 I/O Standard consumes the highest amount of power for the device.

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