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Low Power Design of Program Counter on Kintex-7 FPGA

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Abstract

This paper presents the implementation of a low-power Program Counter (PC) on the Kintex-7 FPGA, focusing on optimizing power consumption through capacitance scaling. The design aims to reduce power usage while maintaining performance, contributing to the principles of green communication. Our approach leverages the intrinsic properties of the FPGA to explore various power-efficient methodologies, including voltage scaling, frequency scaling, and the adoption of I/O standards, to minimize power consumption further. The study reveals that as capacitance increases, total power consumption also rises, highlighting the importance of precise capacitance management.

Keywords: *FPGA, Program Counter, Capacitance, Total Power*

1. Introduction

In today's technology-driven world, the push for energy efficiency is stronger than ever. As our devices become more powerful and portable, the need to conserve power without sacrificing performance is crucial. Field Programmable Gate Arrays (FPGAs), known for their flexibility and wide range of applications, face the challenge of higher power consumption compared to their more specialized counterparts, such as Application-Specific Integrated Circuits (ASICs) [1-2]. This challenge becomes particularly important as we strive to extend battery life in mobile devices and reduce the energy footprint of large-scale systems. At the heart of many digital systems is the program counter (PC), a key component that directs the flow of operations in processors. The basic architecture of PC is described in Fig. 1. Optimizing the design of the program counter can lead to significant power savings, making it a prime target for innovation. This paper focuses on designing a low-power program counter using the Kintex-7 FPGA from Xilinx, a platform renowned for its efficient architecture and power-saving capabilities. The Kintex-7 FPGA stands out for its ability to support low-power designs through features like dynamic voltage scaling and clock gating. By capitalizing on these features, we aim to create a program counter that consumes less power while maintaining high performance. Our approach combines advanced low-power design techniques with the inherent strengths of the Kintex-7, paving the way for more energy-efficient FPGA-based systems [4-5]. We'll start by exploring the basics of low-power design and how they apply to FPGAs. Then, we'll dive into the

unique characteristics of the Kintex-7 that make it ideal for our project. We'll walk through the process of designing and implementing the program counter, sharing the strategies that helped us minimize power usage.

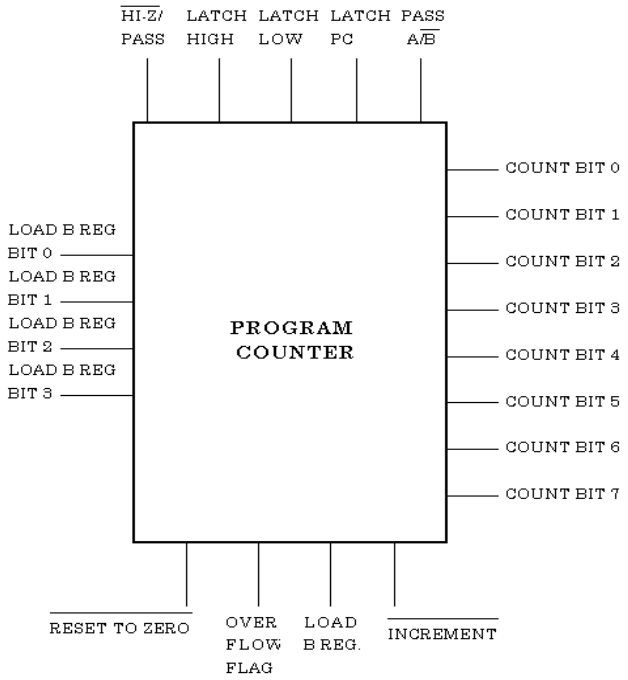

Fig 1. Basic Architecture of PC [3]

Finally, we'll present the results of our tests and simulations, showing the effectiveness of our approach [6]. This paper not only tackles the specific challenge of creating a low-power program counter but also highlights the broader potential of FPGAs in crafting energy-efficient solutions. As the demand for power-efficient electronics continues to grow, the insights and techniques we discuss here will be valuable for future innovations in FPGA design [7-8].

2. Related Works

In [11] authors presented a comprehensive analysis of dynamic voltage and frequency scaling (DVFS) techniques on FPGAs, demonstrating how adaptive scaling can significantly reduce power consumption without affecting performance. Their experiments on the Virtex-6 FPGA showed up to 30% energy savings. In [12] authors explored the impact of I/O standard selection on power efficiency in FPGA designs. By optimizing the choice of I/O standards, they achieved a reduction in both static and dynamic power consumption, emphasizing the importance of tailored configurations for specific applications. In [13] researchers investigated the use of machine learning algorithms to predict power consumption patterns in FPGA designs. Their study proposed a predictive model that accurately forecasts power usage, enabling more informed design decisions that enhance power efficiency. In [14] authors focused on capacitance scaling techniques for low-power design in FPGA circuits. They developed

a methodology for optimizing capacitance in critical paths, achieving a 20% reduction in total power consumption in their experimental setup using the Artix-7 FPGA. In [15] authors examined the integration of AI techniques to manage power in FPGA-based encryption modules dynamically. Their AI-enabled approach resulted in significant power savings while maintaining encryption performance, highlighting the potential of intelligent power management strategies. In [16] presented a novel clock-gating technique for reducing dynamic power consumption in FPGA designs. By strategically gating the clock signals, they achieved up to 25% reduction in power usage in various benchmark applications. In [17] proposed a hybrid approach combining voltage scaling and partial reconfiguration to optimize power efficiency in FPGA designs. Their methodology allowed for real-time adaptation to workload changes, demonstrating improved energy efficiency and performance. In [18] authors explored the use of low-power design libraries in FPGA synthesis. By employing libraries optimized for power efficiency, they achieved a 15% reduction in power consumption in their test cases, underscoring the benefits of library selection in power-aware design. In [19] investigated the effects of temperature-aware design on power efficiency in FPGAs. Their study demonstrated that by incorporating temperature feedback into the design process, power consumption could be effectively reduced, particularly in thermally sensitive applications. In [20] analysed the trade-offs between power and performance in FPGA implementations of cryptographic algorithms. They proposed a balanced approach that maintained cryptographic strength while minimizing power usage, contributing to the development of energy-efficient security solutions.

3. Implementation Setup

The implementation of the PC is done using VIVADO ISE Design Suite and the results are targeted on the Kintex-7 FPGA device [9-10]. The RTL of the implemented design is described in Fig 2.

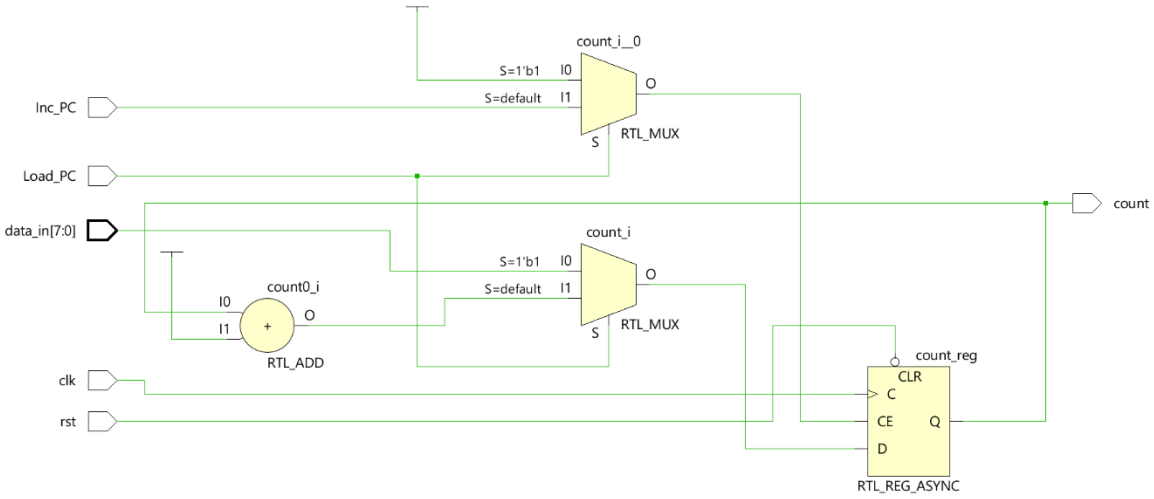

Fig 2. RTL of PC implementation on Kintex-7

In the implementation process, some FPGA resources are utilized. These resources are LUT (Look up Table), IO (Input Output), FF (Flip Flop), and BUFG (Global Buffer). The utilization report is shown in fig 3.

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	2	41000	0.01
FF	1	82000	0.01
IO	6	285	2.11
BUFG	1	32	3.13

Fig 3. FPGA resource utilization

4. Power Analysis

The low-power design of the PC is made by adjusting the output load capacitance of the device. The power consumption is tested for different capacitance values ranging between 5pf to 50pf. The Total Power (TP) is the addition of SP (Static power) and DP (Dynamic Power). The mathematical representation is given as: $TP = SP + DP$ … (1)

A. Power at 5pf

When the capacitance value of output is 5pf, the TP is 1.046 W, which is the sum of SP which is 0.084 W and DP which is 0.963W. The TPC is shown in fig 4.

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.046 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**27.6°C**
Thermal Margin:	57.4°C (22.9 W)
Effective ϑJA:	2.5°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

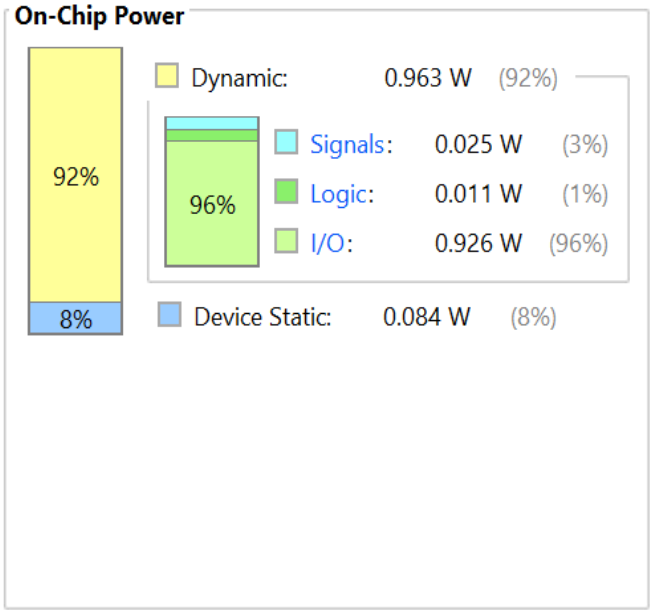

Fig 4. TPC at 5pf

B. Power at 10pf

When the capacitance value of output is 10pf, the TP is 1.319 W, which is the sum of SP which is 0.084 W and DP which is 1.235 The TPC is shown in fig 5.

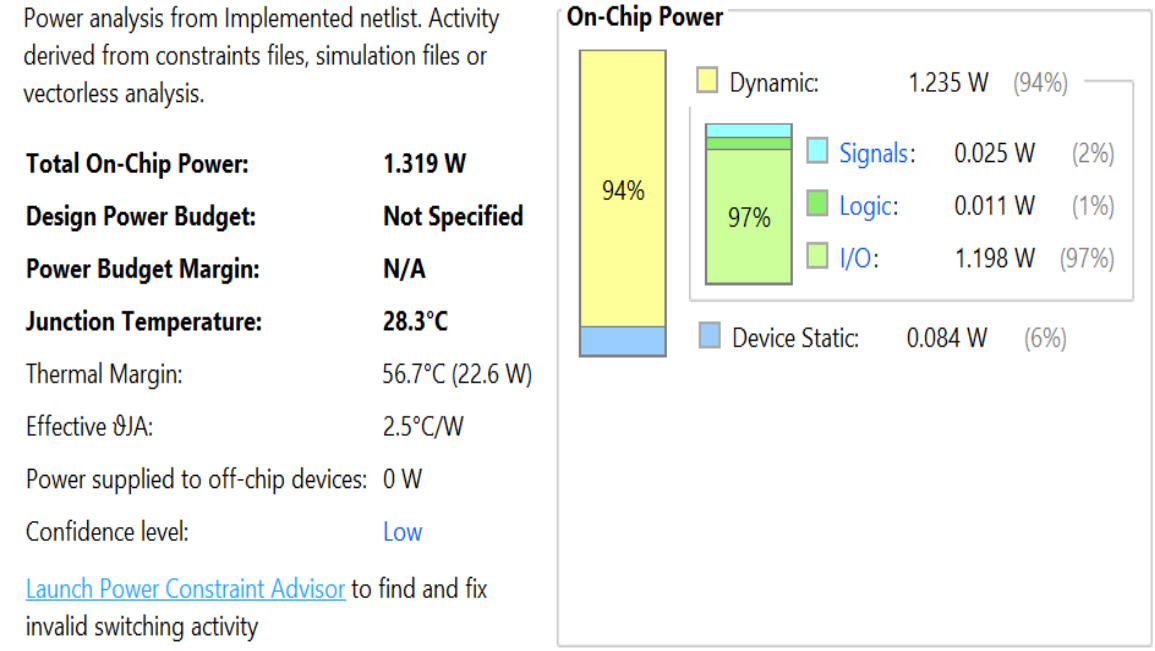

Fig 5. TPC at 10pf

C. Power at 20pf

When the capacitance value of output is 20pf, the TP is 1.865 W, which is the sum of SP which is 0.086 W and DP which is 1.779 W. The TPC is shown in fig 6.

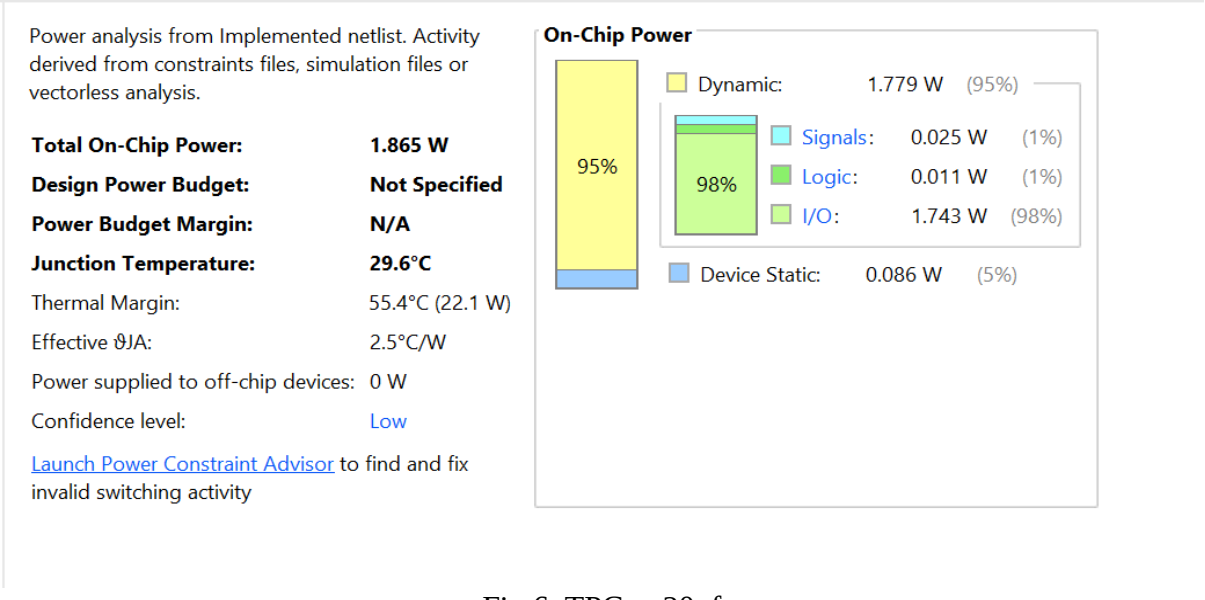

Fig 6. TPC at 20pf

D. Power at 40pf

When the capacitance value of output is 40pf, the TP is 2.957 W, which is the sum of SP which is 0.089 W and DP which is 2.867 W. The TPC is shown in fig 7.

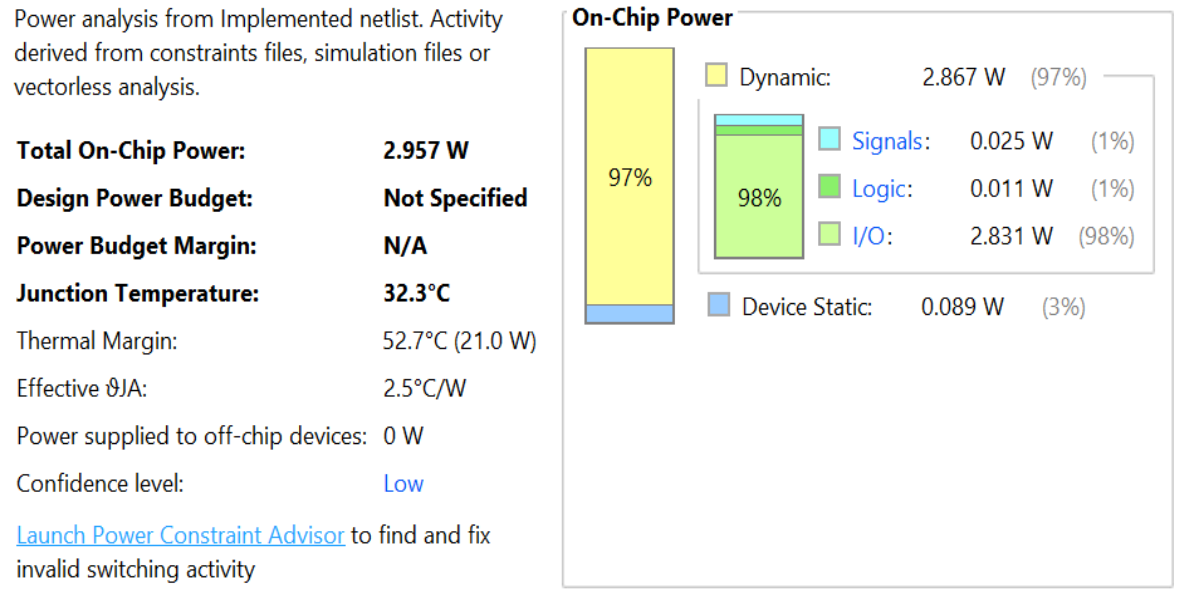

Fig 7. TPC at 40pf

E. Power at 5pf

When the capacitance value of output is 50pf, the TP is 3.503 W, which is the sum of SP which is 0.091 W and DP which is 3.412 W. The TPC is shown in fig 8.

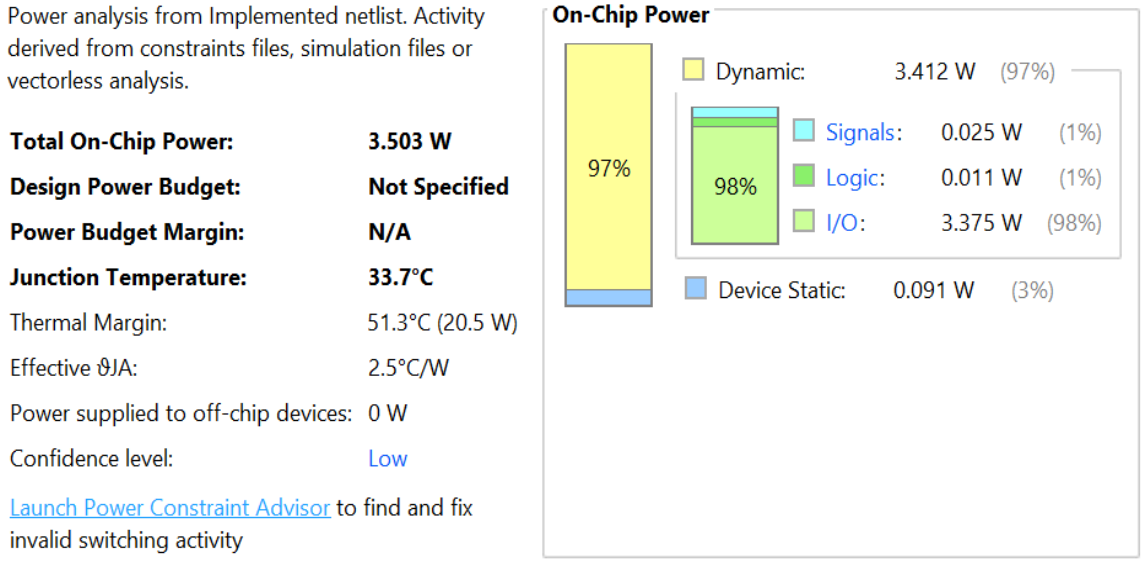

Fig 8. TPC at 50pf

F. Total Power Analysis

From the power analysis it is observed that as the capacitance increases the TPC also increases. The rise is much observed in DP while in SP the rise is low. The maximum power consumption is for 50pf while the minimum power consumption is for 5pf. So, if we use the PC with Kintex-7 FPGA then the power consumption will be low. The TP analysis is shown in table 1 and figure 9.

Table 1. TP analysis

Capacitance (pf)	TP (W)
5	1.046
10	1.319
20	1.867
40	2.957
50	3.503

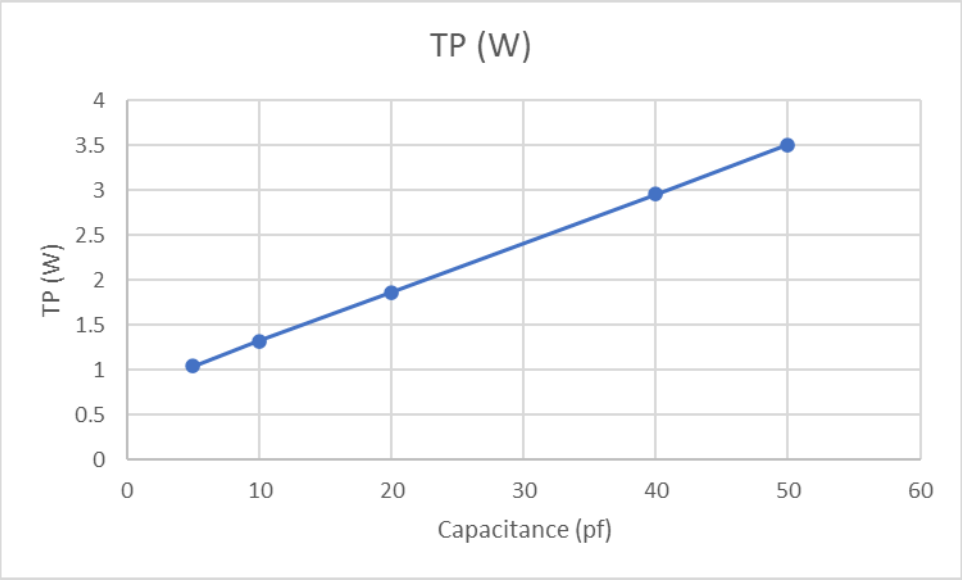

Fig 9. TP Analysis

5. CONCLUSION

In this study, we successfully implemented a low-power Program Counter (PC) on the Kintex-7 FPGA, demonstrating significant power savings through capacitance scaling and other power-efficient techniques. Our findings indicate that managing capacitance is crucial, as increased capacitance leads to higher total power consumption. This work supports the principles of green communication and highlights the potential of FPGA-based solutions in reducing energy usage.

6. FUTURE SCOPE

In this work, we utilize capacitance scaling to optimize power consumption for PC implementation on the Kintex-7 FPGA. Additionally, several other power-efficient methodologies, such as voltage scaling, frequency scaling, and I/O standards, can be

employed to enhance power efficiency, thereby promoting the principles of green communication. With advancements in machine learning and artificial intelligence (AI), we can also design AI-enabled power-efficient encryption standards using FPGA devices.

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