ISSN: 2456-0065 DOI: 10.21058/gjet.2015.1106

Junction Temperature Aware Energy Efficient Router Design on FPGA

Vandana Thind, Shivani Sharma, M H Minwer, D M Akbar Hussain
[1,2]Gyancity Reseach Lab, Gurgaon India
[3]Addalaichenai National College Of Education, Srilanka
[4]Aalborg University, Denmark
vandana@gyancity.com, shalu16sharma@gmail.com, mhminver@gmail.com, akh@et.aau.dk

***Abstract*—Energy, Power and efficiency are very much related to each other. To make any system efficient, Power consumed by it must be minimized or we can say that power dissipation should be less. In our research we tried to make a energy efficient router design on FPGA by varying junction temperature. By varying junction temperature the value of leakage is observed and its effect on total power dissipated is also obtained. This research is made by keeping output load at value 50.The result is also obtained at different frequencies i.e. at 10MHz, 0.1GHz and 1GHz. Different values of output power at observed and reduction the power is calculated accordingly. So this project gives an overview to make the router efficient by varying junction temperature.**

Keywords- *FPGA, Power, Router, Junction Temperature, Energy Efficiency*

I. INTRODUCTION

When we are working with any device it is human tendency that he always wants to make a system which is cheaper. But it is very important to concentrate on its output as well i.e. whether the system is efficient or not. In this paper we have done research on making a router design on FPGA and calculating its power consumptions as well as leakage power at different junction temperatures and different frequencies. First question comes in every mind is what is a router? And what is FPGA? Router is a device which is used to connect different networks continually over a large distance. Router forwards the data packets between the computer networks. Router has following properties and drawbacks.

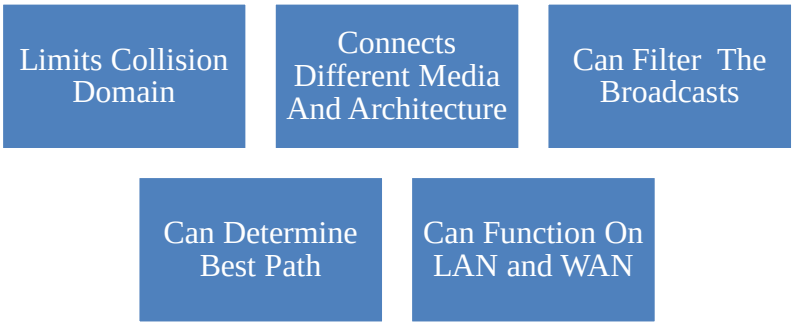

Figure 1: Properties of Router

ISSN: 2456-0065 DOI: 10.21058/gjet.2015.1106

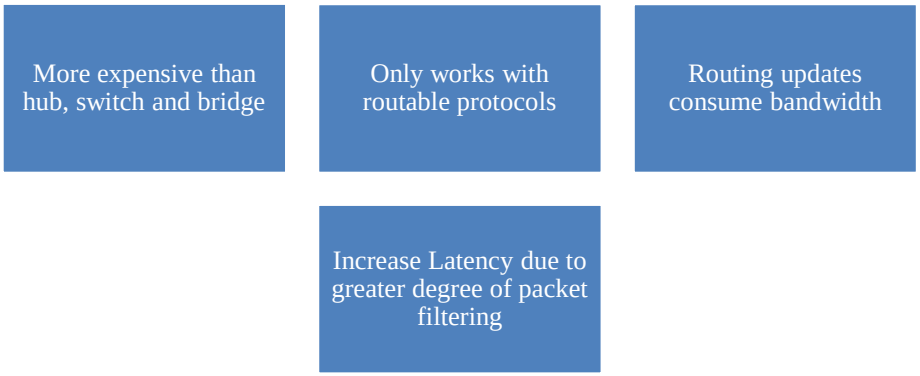

Figure 2: Drawbacks of Router

Field Programmable Gate Arrays i.e. FPGAs are one of the semiconductor devices which are made following a matrix and have configurable logic blocks called CLBs which are connected by programmable interconnects. FPGAs are reprogrammable as per the requirements for their functionality after manufacturing. Software used for analysis is Xilinx which enables the developer to synthesize the design as well as simulate the output.

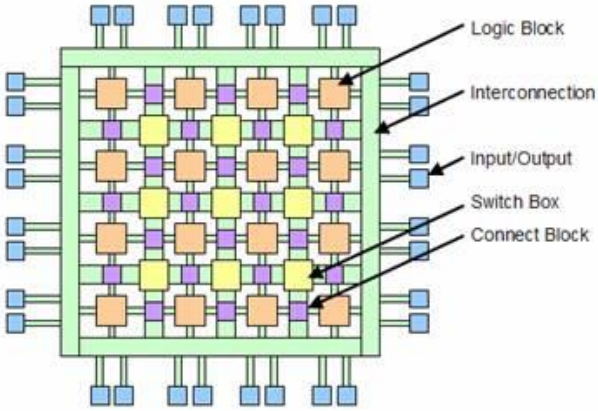

Figure 3: Basic architecture of FPGA [4]

FPGA have programmable nature and hence they are ideally fit in markets. Xilinx is industry leader that provides comprehensive solutions that are consist of different FPGA devices as well as ready to use IP cores and advanced software [5].

II. RELATED WORK

There can be various techniques through which efficiency can be increased or power dissipation can be reduced. It can be achieved either by varying capacitance, temperature or many other variables. This research strictly emphasizes on increasing efficiency by varying junction temperature at various frequencies.

2.1Power efficient approach and performance control for Routers [1]

This paper also focus on less power consumption and an efficient approach for designing routers but in our research this is achieved by varying junction temperature at different frequencies and noting down the respective values of power dissipated, where as mentioned related paper has two aspects that are dynamic performance control and static performance control. They worked on power cutting technology and a mode of power according to frequency switching.

ISSN: 2456-0065 DOI: 10.21058/gjet.2015.1106

2.2 Thermal aware global routing of Very large scale integration chips for enhanced reliability [2]

This paper relates the effect of temperature on mean time to failure of interconnects. They purposed a thermal aware global router which can reduce the probability of failure of the chip. Our paper relates the temperature with router efficiency which is related to the power consumption. This also approaches to make a thermal aware router but on FPGA. Junction temperature is varied and analysis is done on different frequencies to note down the total reduction in power consumption and leakage also.

2.3Efficient circuit clustering for area and Power reduction in Field Programmable Gate Array [3]

Above mentioned paper has used Xilinx as well. This is based on the dynamic power consumption in FPGAs as they consume more power and also on reduction of area but there is no relation with junction temperature. We also want to reduce as much power as possible but we have achieved this by varying junction temperature which is a major difference between two papers. They reduced the area of devices and provide an efficient seed selection method to reduce average track count.

2.4 Generic Low-Latency Network On Chip Router Architecture for Field Programmable Gate Array Computing Systems [6]

A router that is cost effective as well as have low latency for packet-switched Network On Chip designs, custom made for Field Programmable Gate Array, was conferred. [6] Above mentioned paper is designed to a level so that it can totally exploit the properties of and constraints of Field Programmable Gate Array. It is totally different from our power efficient router design but is based on designing a cost effective as well as low latency router tailored for FPGA.

2.5 A Fast Routability Driven Router for FPGAs [7]

This paper presents a fast driven router for FPGA. The router is of specific interest to users who are ready to take delicately results of lower quality in place of very small routing times. [7]. Along with, there are many more techniques used to make energy efficient design like Energy Efficient and Thermal Aware Object Tracking on FPGA [8], Energy Efficient FIR Filter for Digital Signal Processing [9], Energy Efficient ROM Design on FPGA [10], Energy Efficient Portable ALU Design on FPGA [11], SSTL Based Energy Efficient ISCAS'99 Benchmark Circuit Design [12], Energy Efficient RAM Design on 40nm and 65nm FPGA [13], Energy Efficient Multiplier Design [14], Green Communication Using Fibonacci Generator Design on FPGA [15], Power Efficient Implementation of DES Security Algorithm [16], CTHS Based Energy Efficient Thermal Aware Image ALU [17] and Energy Efficient Encoder Design for security [18].

III. DATA ANALYSIS AND INTERPRETATION

A. Results on 10 MHz

Table 1: Power Dissipation of Router For 0-26.5^{o}C Junction Temperature

Temperature	26.5^{o}C	20^{o}C	15^{o}C	5^{o}C	0 ^{o}C
Leakage	0.541	0.506	0.481	0.435	0.415

ISSN: 2456-0065 DOI: 10.21058/gjet.2015.1106

Total Power	0.628	0.593	0.568	0.522	0.502

There is 4.49%, 13.72%, 17.98% and 23.29% fall in the leakage power when temperature is scaled down from 26.5ºC to 20ºC, 15ºC, 5ºC, 0ºC respectively.
There is 5.57%, 9.57%, 16.87% and 23.29% fall in the total power when temperature is scaled down from 26.5ºC to 20ºC, 15ºC, 5ºC, 0ºC respectively.

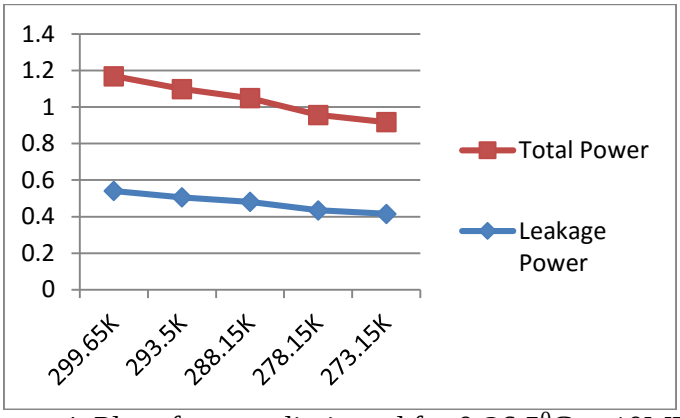

Figure 4: Plot of power dissipated for 0-26.5^{0}C at 10MHz

Table 2: Power Dissipation of Router For 40-125ºC Junction Temperature

Temperature	40ºC	50ºC	60ºC	70ºC	125ºC
Leakage	0.623	0.694	0.775	0.867	1.029
Total Power	0.710	0.781	0.862	0.954	1.116

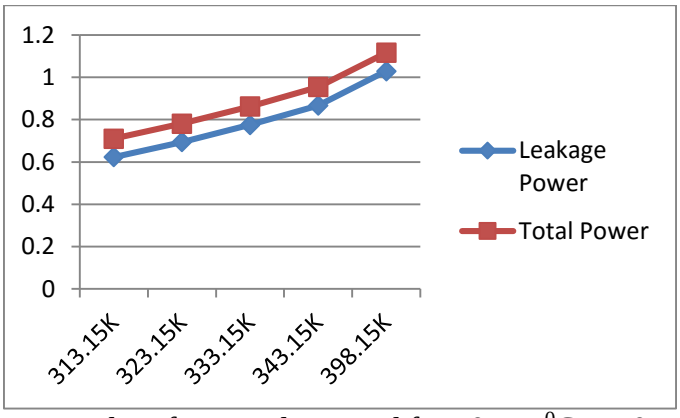

Figure 5: Plot of power dissipated for 40-125^{0}C at 10MHz

There is 39.45%, 32.55%, 24.68% and 15.74% fall in the leakage power when temperature is scaled down from 125ºC to 40ºC, 50ºC, 60ºC, 70ºC respectively.
There is 36.37%, 30.01%, 22.75% and 14.51% fall in the total power when temperature is scaled down from 125ºC to 40ºC, 50ºC, 60ºC, 70ºC respectively

B. Results on 0.1 GHz

Table 3: Power Dissipation of Router For 0-26.5ºC Junction Temperature

Temperature	26.5^{0}C	20ºC	15ºC	5ºC	0 ºC
Leakage	0.541	0.506	0.481	0.435	0.415
Total power	1.411	1.376	1.351	1.305	1.285

ISSN: 2456-0065 DOI: 10.21058/gjet.2015.1106

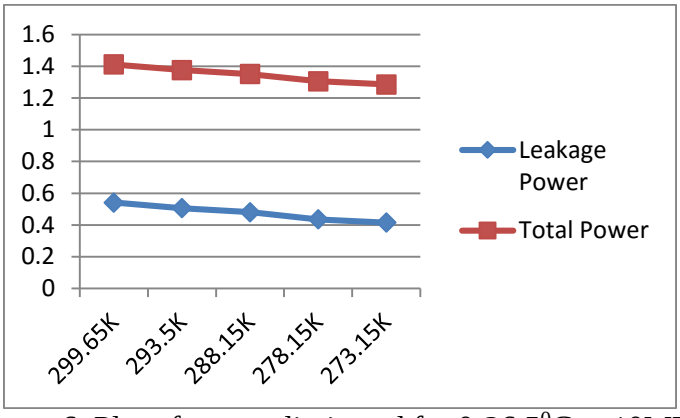

Figure 6: Plot of power dissipated for 0-26.5^{0}C at 10MHz

There is 2.48%, 4.25%, 7.51% and 8.92% fall in the total power when temperature is scaled down from 26.5ºC to 20ºC, 15ºC, 5ºC, 0ºC respectively.

Table 4: Power Dissipation of Router For 40-125ºC Junction Temperature

Temperature	40^{0}C	50ºC	60ºC	70ºC	125ºC
Leakage	0.623	0.694	0.775	0.867	1.029
Total Power	1.463	1.565	1.645	1.737	1.899

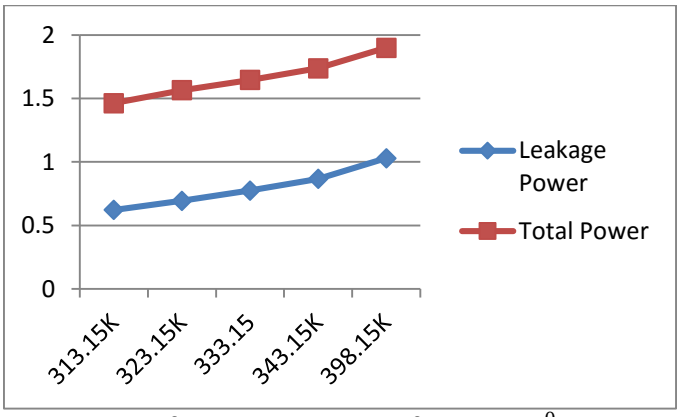

Figure 7: Plot of power dissipated for 40-125^{0}C at 10MHz

There is 22.95%, 17.58%, 13.37 % and 8.53% fall in the total power when temperature is scaled down from 125ºC to 40ºC, 50ºC, 60ºC, 70ºC respectively.

C. Results on 1 GHz

Table 5: Power Dissipation of Router For 0-26.5ºC Junction Temperature

Temperature	26.5^{0}C	20ºC	15ºC	5ºC	0ºC
Leakage	0.541	0.546	0.481	0.435	0.415
Total power	9.243	9.208	9.183	9.137	9.116

ISSN: 2456-0065 DOI: 10.21058/gjet.2015.1106

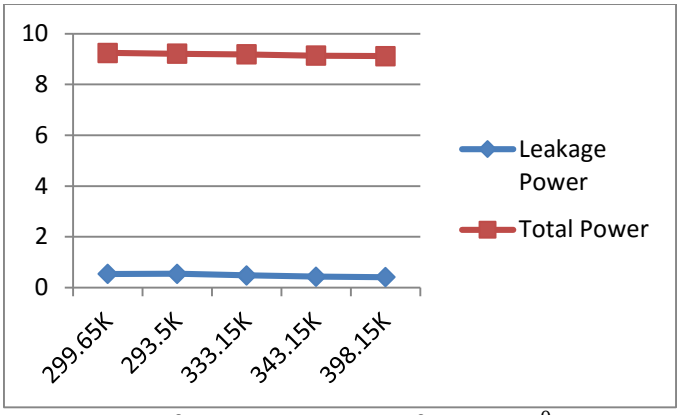

Figure 8: Plot of power dissipated for 0-26.5^{0}C at 10MHz

There is 0.37%, 0.64%, 1.14% and 1.37% fall in the total power when temperature is scaled down from 26.5^{o}C to 20^{o}C, 15^{o}C, 5^{o}C, 0^{o}C respectively.

Table 6**:** Power Dissipation of Router For 40-125^{o}C Junction Temperature

Temperature	40^{o}C	50^{o}C	60^{o}C	70^{o}C	125^{o}C
Leakage	0.623	0.694	0.775	0.867	1.029
Total Power	9.325	9.396	9.477	9.569	9.731

There is 4.17%, 3.44%, 2.61 % and 1.66% fall in the total power when temperature is scaled down from 125^{o}C to 40^{o}C, 50^{o}C, 60^{o}C, 70^{o}C respectively

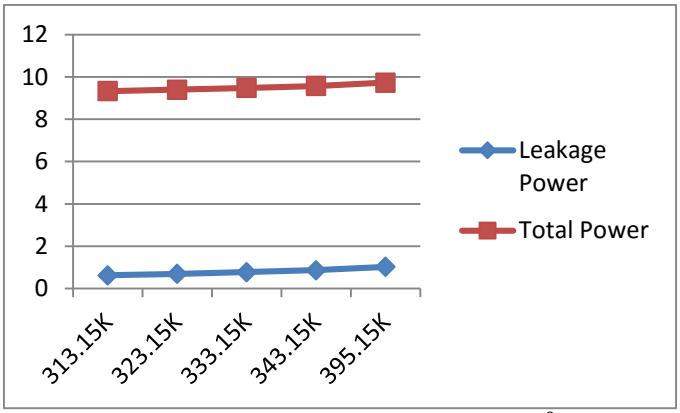

Figure 9: Plot of power dissipated for 40-125^{0}C at 10MHz

IV. CONCLUSION

Our research is done precisely which leads to designing of an energy efficient router on FPGA. It can be clearly seen from results that as we are varying junction temperature there is variation in the total power dissipated as well as leakage power. So junction temperature plays significant role in the total power consumed. As we are focusing on designing of efficient router, power is the major aspect related to efficiency. Reduction in total power at different temperatures is observed accurately.

V. FUTURESCOPE

Our approach is to design energy efficient router on FPGA but in future bridge can also be designed efficiently by varying different parameters. The frequency range used by us can also be varied and this may also provide us with better results. We have used Virtex-6.Further Virtex-7 and System-On-Chip can be used to enhance the power

ISSN: 2456-0065 DOI: 10.21058/gjet.2015.1106

consumption and leakage.3-D FPGA designing can also be used in future. There will be enough uses of router with less power consumption and it will make system much cheaper.

REFRENCES

[1]. M. Oulmahdi.; C. Chassot, .; E. Exposito "An energy-aware TCP for multimedia streaming", *Smart Communications in Network Technologies, 2013 International Conference on,* Pp: 1 - 5 Volume: 01, 17-19 June 2013

[2]. A. Gupta "Thermal aware global routing of Very Large Scale Integration chips for enhanced reliability." *Quality Electronic Design,9th International Symposium on*. IEEE, 2008.

[3]. A. Singh, G. Parthasarathy, and M. M. Sadowska. "Efficient circuit clustering for area and power reduction in Field Programmable Gate Arrays." *ACM Transactions on Design Automation of Electronic Systems* , 2002 Pp: 643-663.

[4]. Basic architecture of FPGA accessible at: http://ca.olin.edu/2005/fpga_dsp/fpga.html

[5]. FPGA Applications accessible at: http://www.xilinx.com/fpga/

[6]. L. Y. J. McCanny, and S. Sezer. "Generic low-latency noc router architecture for Field Programmable Gate Array computing system , IEEE,2011.

[7]. S. ,Jordan S. ,V.Betz, and J. Rose."A Fast routability driven router for Field Programmable Gate Array." Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field Programmable Gate Array .ACM,1998.

[8]. S.H.A. Musavi, B. S. Chowdhry, T. Kumar, B. Pandey, W.Kumar, "IoTs Enable Active Contour Modeling Based Energy Efficient and Thermal Aware Object Tracking on FPGA", **Springer** Wireless Personal Communications, ISSN:1572-834X(electronic), SCI Indexed, Vol.82, No.3, pp.1-15, 20 May 2015

[9]. B.Pandey, T. Kumar, T. Das and J. Kumar "Thermal Mechanics Based Energy Efficient FIR Filter for Digital Signal Processing", AMM Journal, vol. 612, pp. 65-70, August 2014.

[10]. R. Saini, N. Bansal, M. Bansal, L. Kalra, B. Pandey and D. M. A. Hussain, "Ambient Temperature Based Thermal Aware Energy Efficient ROM Design on FPGA", Advanced Materials Research, Trans Tech Publications, pp.467-470

[11]. Tanesh Kumar, Bishwajeet Pandey, Teerath Das, and Bhavani Shankar Chowdhry, "Mobile DDR IO Standard Based High Performance Energy Efficient Portable ALU Design on FPGA", Springer Wireless Personal Communications, An International Journal, Volume 76, Issue 3 (2014), Page 569-578, (SCI Indexed),

[12]. Amanpreet Kaur, Bishwajeet Pandey, Sunny Singh, Aditi Modgil, and Kanika Garg, "SSTL Based Energy Efficient ISCAS'99 Benchmark Circuit Design on FPGA", International Journal of Energy, Information and Communications, Vol.6, Issue 3 (2015), pp.39-46, http://www.sersc.org/journals/IJEIC/vol6_Is3/5.pdf

[13]. Aditi Moudgil, Kanika Garg, Bishwajeet Pandey, "Low Voltage Complementary Metal Oxide Semiconductor Based Internet of Things Enable Energy Efficient RAM Design on 40nm and 65nm FPGA", International Journal of Smart Home, Vol. 9, No.9, pp.37-50, September 2015. http://www.sersc.org/journals/IJSH/vol9_no9_2015/5.pdf

[14]. Shivani Madhok, Bishwajeet Pandey, Amanpreet Kaur, D M Akbar Hussain, Mohamed Hashim Minver, "HSTL IO Standard Based Energy Efficient Multiplier Design using Nikhilam Navatashcaramam Dashatah on 28nm FPGA", International Journal of Control and Automation, Vol.8, No.8, August 2015. http://www.sersc.org/journals/IJCA/vol8_no8/5.pdf

[15]. Sumita Nagah, Bishwajeet Pandey, Kartik Kalia, Ravinder Kaur, Md. Saifur Rahman Mahbub-E-Noor, "I/O Standards Based on Green Communication Using Fibonacci Generator Design on FPGA", International Journal of Control and Automation, Vol.8, No.8, August 2015. http://www.sersc.org/journals/IJCA/vol8_no8/13.pdf

[16]. Bishwajeet Pandey, Vandana Thind, Simran Kaur Sandhu, Tamanna Walia, Sumit Sharma , "SSTL Based Power Efficient Implementation of DES Security Algorithm on 28nm FPGA", International Journal of Security and Its Application, Vol.9, No.7, July 2015, pp.267-274, http://www.sersc.org/journals/IJSIA/vol9_no7_2015/23.pdf

[17]. Tanesh Kumar, Bishwajeet Pandey, Sayed Hyder Abbas Musavi, Noor Zaman,"CTHS Based Energy Efficient Thermal Aware Image ALU Design on FPGA", Springer Wireless Personal Communications, An International Journal, ISSN:0929-6212(print), ISSN:1572-834X(electronic), SCI Indexed, Vol.83, No.1, July 2015. http://link.springer.com/article/10.1007/s11277-015-2801-8

ISSN: 2456-0065 DOI: 10.21058/gjet.2015.1106

[18]. Deepa Singh, Kanika Garg, Ravneet Singh, Bishwajeet Pandey, Kartik Kalia, Hasmatullah Noori, "Thermal aware Internet of Things Enable Energy Efficient Encoder Design for security on FPGA", International Journal of Security and Its Applications, Vol.9, No.6, pp. 271-278, June 2015. http://www.sersc.org/journals/IJSIA/vol9_no6_2015/26.pdf