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Energy Power Efficient Vedic Multiplier Design on 28nm FPGA Using Vedic Formula ANURPYENA

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Abstract: The paper is about the designing of the low power energy proficient Vedic multiplier on 28nm field programmable gate array. Our motive here is to design a low power energy efficient design and for that reason, we are doing our study on different types of LVCMOS IO standards: LVCMOS_15, LVCMOS_18, LVCMOS_25, LVCMOS_33. To verify the thermal aware design we have taken 5 different temperatures from five different areas 10ºC, 25ºC, 40ºC, 55ºC, 70ºC. There is 3.73%, 3.21%, 3.005%, 3.002% reduction in leakage power, there is 0.544%,0.71%,3.63%,1.21% reduction in MAT and there is 73.74%,70.43%,52.00%,61.93% reduction in JT for LVCMOS_15, LVCMOS_18, LVCMOS_33, LVCMOS_25 correspondingly as we level down ambient temperature from 70 ºC to 10 ºC.

KEYWORDS : — Vedic Math's, Low Power, Multiplier, Energy Efficient, FPGA.

I. INTRODUCTION

Multiplication is one of the most imperative hardware chunk in any Digital system in order to perform different operations like frequency filtering, frequency transformation and many other. Some of the major arithmetical operations by the multiplier in the Digital systems are to multiply and accrue. Apart from digital systems, it is a vital wedge in Image Processing systems, Arithmetic and Logical Unit of the processors etc. The former processors were not having a Multiplier block, instead they used multiply routines. However with the enhanced levels of amalgamation in the newest VLSI circuits gradually, the chore of conniving a multiplier block has begin getting enormous fidelity in the devise of digital systems. An additional trait of the multiplier which should be given a lot of anxiety in conniving of the system is Power debauchery. A towering throughput and high performance energy efficient multiplier for the Field Programmable Gate Array (FPGAs) is being proposed in this paper. IO standard play a significant role in power dissipation of design. For that cause, we are going to choose the most energy proficient IO standards in LVCMOS family they are LVCMOS15, LVCMOS18, LVCMOS25 and LVCMOS33. To scrutinize the transformation in this electronic + arithmetic design made on changing the ambient temperature [4-7] i.e. to verify the thermal aware design we have taken 5 different temperatures from five different areas. The key feature of this projected design is that it is based on "Ancient Indian Vedic Mathematics". This paper tells of “Anurpyena Sutra” which can increase the speed of multiplier by reducing the number of repetitions.

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Anurpyena : The upa-sutra 'ANURPYENA' means proportionality. This sutra is extremely helpful to find products of two numbers when both of them are near the common bases that is powers of base 10

Example:

In this Method we will take 50 as our working again, and we will take it as 5 x 10 = 50. We write the numbers out, all along with their differences from our operational base (50).

42 -8

48 -2

We cross add/subtract to get 40 .This time however, since we are treating it as 5 x 10 = 50…we multiply 40 x 5. When we do this we get 200.

42 -8

48 -2

200 /

Since we took this as 5 x 10, our right-hand side can only have one digit (there's only one zero in 10). So we multiply (-8) x (-2) = 16, and this becomes our right-hand side.

42 -8

48 -2

200 / 16

Answer: 42 x 48 = 2016.

II. Analysis of Maximum Ambient Temperature and Junction Temperature

A. Analysis of MAT, Junction temperature and Leakage power for various IO standards

Table 1:Analysis of MAT ,JT, LP for LVCMOS_18 IO standard

	MAT	JT	POWER
10ºC	69.6	25.4	7.517
25 ºC	69.5	40.5	7.537
40 ºC	69.5	55.5	7.576
55 ºC	69.3	70.7	7.647
70 ºC	69.1	85.9	7.767

There is 0.71%, 70.43%,3.21% reduction in MAT,JT,POWER respectively when we scale down ambient temperature from 70 ºC to 10 ºC for LVCMOS_18 IO standard.

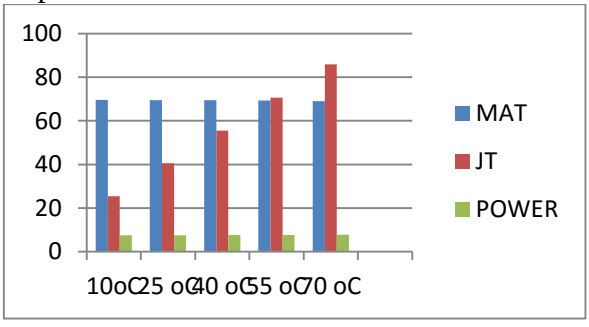

Figure 1:Graphical representation of MAT, JT, LP for LVCMOS_18

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Table 2:Analysis of MAT ,JT,LP for LVCMOS_25 IO standard

	MAT	JT	POWER
10°C	57.7	37.3	13.288
25 °C	57.7	52.3	13.322
40 °C	57.5	67.5	13.385
55 °C	57.3	82.7	13.493
70 °C	57.0	98.0	13.699

There is 1.21%, 61.93%,3.002% reduction in MAT,JT,POWER when we range down ambient temperature from 70 ^{0} to 10 ^{0}C.

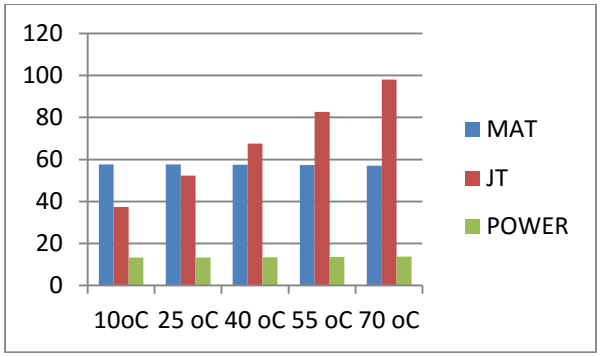

Figure 2: Graphical representation of MAT, JT, LP for LVCMOS_25

Table 3: Analysis of MAT, JT, LP for LVCMOS_33 IO Standard

	MAT	JT	POWER
10°C	38.5	56.5	22.658
25 °C	38.4	71.6	22.731
40 °C	38.1	86.9	22.855
55 °C	37.7	102.3	23.055
70 °C	37.1	117.9	23.360

There is 3.63%,52.00%,3.005% reduction in MAT,JT,POWER when we range down temperature from 70 ^{0}C to 10 ^{0}C.

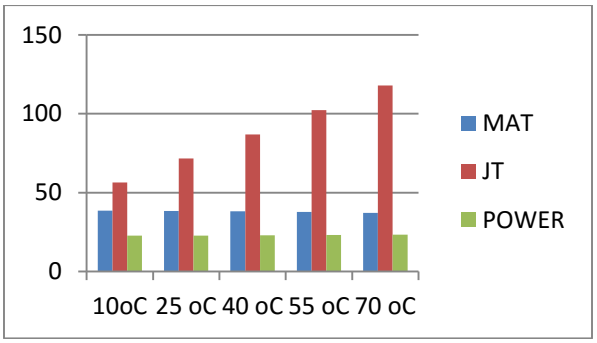

Figure 3: Graphical representation of MAT, JT, and LP for LVCMOS_33

Table 4: Analysis of MAT, JT, and LP for LVCMOS_15 IO standard

	MAT	JT	POWER
10°C	73.5	21.5	5.598
25 °C	73.5	36.5	5.616
40 °C	73.4	51.6	5.649
55 °C	73.3	66.7	5.710

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70 °C	73.1	81.9	5.815

There is 0.544%, 73.74%, 3.73% reduction in MAT, JT, and POWER respectively when we range down ambient temperature from 70 °C to 10 °C

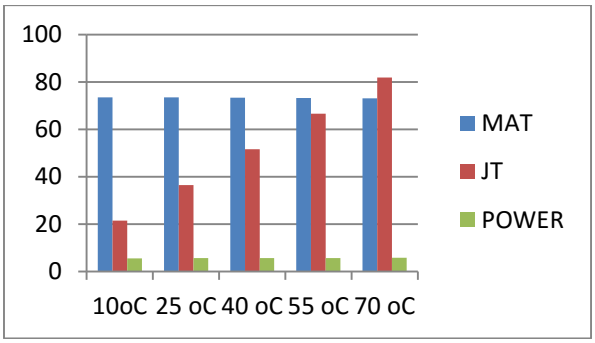

Figure 4: Graphical representation of MAT, JT, LP for LVCMOS_15

III. **RESULTS**

A. POWER ANALYSIS

Table 5: Leakage Power analysis for various IO standards

	Lvcmos15	Lvcmos18	Lvcmos33	Lvcmos25
10 °C	5.598	7.517	22.658	13.288
25 °C	5.616	7.537	22.731	13.322
40 °C	5.649	7.576	22.855	13.385
55 °C	5.710	7.647	23.055	13.493
70 °C	5.815	7.767	23.360	13.699

There is 3.73%,3.21%,3.005%,3.002% reduction in leakage power for LVCMOS_15, LVCMOS_18, LVCMOS_33, LVCMOS_25 respectively when we scale down ambient temperature from 70° C to 10 ° C

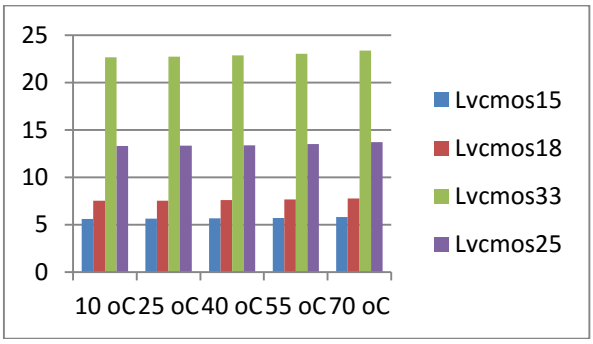

Figure 5: Graphical Power analysis for various IO standards

B. THERMAL ANALYSIS

Table 6: Thermal Analysis in terms of MAT for various IO standards

	Lvcmos15	Lvcmos18	Lvcmos33	Lvcmos25
10 °C	73.5	69.6	38.5	57.7
25 °C	73.5	69.5	38.4	57.7
40 °C	73.4	69.5	38.1	57.5
55 °C	73.3	69.3	37.7	57.3
70 °C	73.1	69.1	37.1	57.0

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There is 0.544%,0.71%,3.63%,1.21% reduction in MAT for LVCMOS_15, LVCMOS_18, LVCMOS_33, LVCMOS_25 respectively when we range down ambient temperature from 70^0C to 10^0C.

Table 7: Thermal Analysis in terms of JT for various IO standards

	Lvcmos15	Lvcmos18	Lvcmos33	Lvcmos25
10 °C	21.5	25.4	56.5	37.3
25 °C	36.5	40.5	71.6	52.3
40 °C	51.6	55.5	86.9	67.5
55 °C	66.7	70.7	102.3	82.7
70 °C	81.9	85.9	117.9	98.0

There is 73.74%,70.43%,52.00%,61.93% reduction in JT for LVCMOS_15, LVCMOS_18, LVCMOS_33, LVCMOS_25 respectively when we range down ambient temperature from 70^0C to 10^0C.

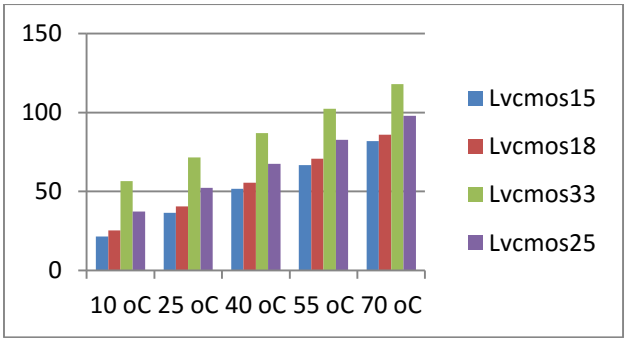

Figure 6: Graphical Thermal analysis for various IO standards

III. CONCLUSION

Low Power Energy efficient Vedic multiplier design is possible with LVCMOS I/O standard. Variation in ambient temperature will create a significant variation in Junction temperature. But, there only a gradual change in MAT and LP with change in temperature for uniform IO standard. There is 3.73%, 3.21%, 3.005%, 3.002% reduction in leakage power, there is 0.544%,0.71%,3.63%,1.21% reduction in MAT and there is 73.74%,70.43%,52.00%,61.93% reduction in JT for LVCMOS_15, LVCMOS_18, LVCMOS_33, LVCMOS_25 respectively when we range down ambient temperature from 70^0C to 10^0C.

IV. FUTURE SCOPE

By moving from one IO standard LVCMOS to others such as HSTL or HSTL_DCI or SSTL or LVDCI or HSLVDCI, we can discover new alternative to decrease power debauchery. Power debauchery is certain to diverge with various IO standards and the reason after that. This is Kintex-7 based on 28 nm FPGA. There is a wide area to explore this design in latest FPGA's such as Virtex-7, it is based on 28- nm FPGA which makes us proficient to obtain the advantage of deeper sub-micron circuit.

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