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Temperature Sensing Based Energy Efficient Vedic Multiplier Design Using Either Proportionality or Similarity

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***Abstract*— In this project, an innovative design of energy efficient Vedic Multiplier using a prehistoric Vedic mathematics method known as "Anurupyena Shunyamanyat" have been implemented on FPGA. Anurupyena Shunyamanyat is a Sanskrit name which in simple words means ' proportionality 'or ' similarly '. This Sutra is highly useful to find products of two numbers when both of them are near the frequent bases like 10, 50, 500 etc (multiples of powers of 10). Lesser time and energy efficient is today's world demand. Choice of IO Standard plays a very important role in power indulgence design. So, we have selected most energy efficient IO standard Low Voltage Complementary Metal Oxide Semiconductor also called LVCMOS. Then, we try to achieve more energy efficiency with different technology (40nm and 28nm) based FPGA. Virtex-6 and Kintex-7 are the platforms which have been used in this project. In our paper we have implemented our code on Xilinx ISE Design Suite 14.2 were tested on 28nm and 40nm FPGA. In this project we have observed approx 87-88% decrease in leakage power dissipation when we shift from 40nm to 28nm technology based FPGA.**

Keywords* - *Anurupyena Shunyamanyat, Vedic mathematics, FGPA, Energy Efficient, LVCMOS, Virtex, Kintex

I. INTRODUCTION

Low Voltage Complementary Metal Oxide Semiconductor also called LVCMOS and Low Voltage Digitally Controlled Impedance also called LVDCI are the most commonly used IO Standard available on FPGA. High Speed Transceiver Logic also called HSTL, Stub Series Terminated Logic called SSTL and Transistor-Transistor Logic called TTL are few more IO Standards available on FPGA. Our Energy efficient Vedic multiplier [1-8] design is implemented on 40nm Virtex-6 and 28nm Virtex-7 FPGA. Vedic mathematics deals with a range of Vedic mathematical sutra and their applications to carry out tedious and cumbersome arithmetic operations [2]. Other researchers have also performed their research work in the field of Vedic mathematics like implementation of 4*4 multiplier using Urdhva-Tiryakbhyam in 45nm technology[3], another division architecture using another Vedic technique

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known as 'Dhwajam'[4]. A design of an 8 bit fixed point, asynchronous Vedic DSP processor core has also been studied [5]. One of the more silicon-intensive functions which is Multiplication, especially when implemented in Programmable Logic [6]. Many high performance systems such as FIR filters, Digital Signal Processing (DSP), Microprocessors etc have multipliers as the key gears or component.

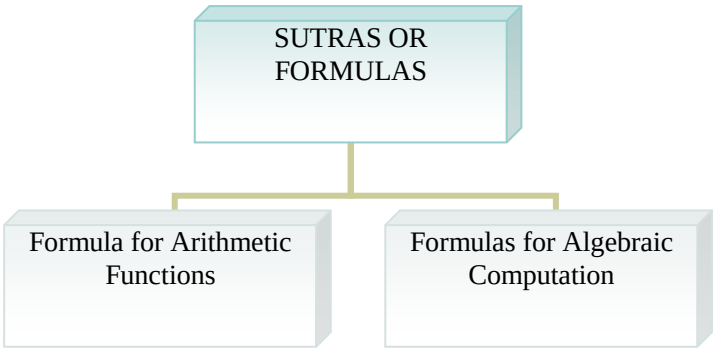

Figure 1: Types of Sutra in Vedic Mathematics

Vedic Mathematics has been divided into two categories, one is the formula for Arithmetic Functions and another one is formula for Algebraic Computation, as shown in Figure1.

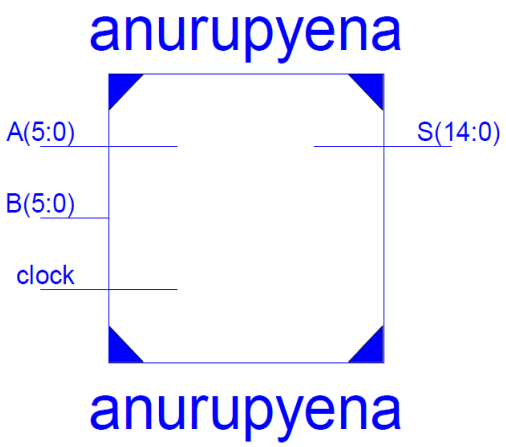

Figure 2**:** Top Level Schematic of Anurupyena Shunyamanyat Sutra

The Top Level Schematic of Anurupyena Shunyamanyat Sutra Based Vedic Multiplier is shown in Figure 2. The Vedic Multiplier is having three inputs and one output. This formula is highly useful in finding products of two numbers when both of them are near the familiar base example 50, 60, 200 etc. For example, 46 (8'b00101110) is the first input and is to be multiplied by 43 (8'b00101011). Both the inputs are nearer to the base 50 and the output will be equal to 1978 (15'b000011110111010). This project deals with Anurupyena, which is a Sanskrit name means proportionality or similarity. In this paper, a Vedic multiplier is intended using Anurupyena. Implementation has been done in Xilinx ISE Design Suite 14.2 and tested on 28nm and 40nm FPGA platform.

Technologies used on FPGA

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40nm and 28nm

Temperature and IO Standard

50ºC, 40ºC and 23.3ºC

Figure 3: Design Parameters in Energy Efficient Vedic Multiplier

Design Parameter for energy efficient Vedic Multiplier has been shown in Figure 3. In this project, different technologies have been used for the purpose of reducing power 40nm and 28nm FPGA platform has been taken into consideration for testing purpose. Temperature is the major factor for the reduction in power of multiplier. Testing is done on different temperatures.

II. SIMULATION

This Waveform is created by using ISim simulator. ISim produce waveform based on 'test bench' generated in Xilinx ISE tool. ISim conjure up behavioral model of the Vedic multiplier.

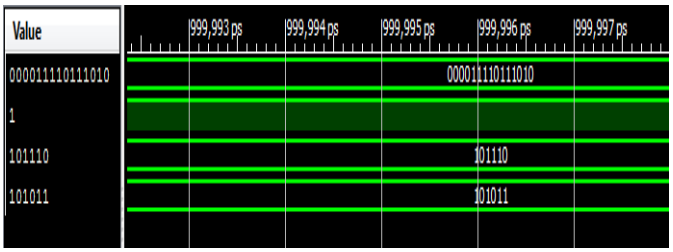

Figure 4: Test bench of Anurupyena

As shown in Fig.4 the waveform which is called testbench in case of Verilog is basically used for testing the outputs of the code. A and B are the two inputs in which A is 46 (101110) whereas B is equal to 43 (101011) one more input has been used i.e. the clock input which is used to provide clock pulse. Therefore, after Multiplication output S is equal to 1978 (000011110111010).

III. RESULTS

Using LVCMOS IO Standard on different Technologies 40nm and 28nm comparisons have been done. In 40nm technology based Virtex-6 FPGA; LVCMOS25 is the uppermost power consumer whereas LVCMOS25 is the least power consumer. LVCMOS25 IO standard belongs to the least power consumer in CMOS logic family. Whereas, in case of Kintex-7, LVCMOS25 consumes the lowest power where LVCMOS15 having more power dissipation. Our main purpose is to find the most energy efficient IO Standard [7].

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A. Power Analysis on 50 Degree Celsius

TABLE 1: Total Power Dissipation Using LVCMOS on 50°C

	40nm	28nm
LVCMOS12	1.291	0.598
LVCMOS15	1.292	0.088
LVCMOS25	1.293	0.046

While using 28nm FPGA, there are 53.67%, 93.18% and 96.4% diminution in total power indulgence of Vedic multiplier using LVCMOS12, LVCMOS15 and LVCMOS25 respectively as shown in Table 1 and Figure 5.

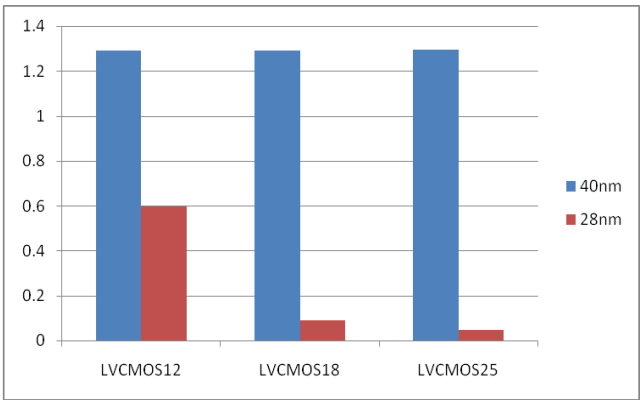

Figure 5: Total Power Dissipation on 50°C Ambient Temperature

B. Power Analysis on 40 Degree Celsius

TABLE 2: Total Power Dissipation Using LVCMOS on 40°C

	40nm	**28nm**
LVCMOS12	1.215	0.574
LVCMOS15	1.216	0.065
LVCMOS25	1.217	0.066

When we use 28nm FPGA, there are 52.7%, 94.6% and 94.5% fall in total power dissipation using 40°C Ambient Temperature for multiplier using LVCMOS12, LVCMOS15 and LVCMOS25 IO Standard respectively as shown in Table 2 and Fig 6.

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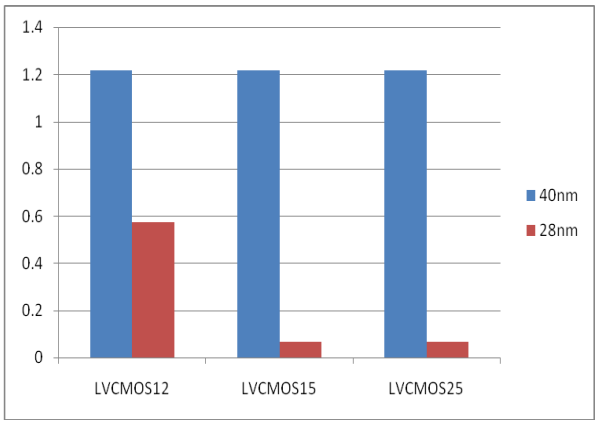

Figure 6: Total Power Dissipation on 40ºC Ambient Temperature

C. Power Analysis on 23.3 Degree Celsius

TABLE 3: Total Power Dissipation Using LVCMOS on 23.3ºC

	40nm	**28nm**
LVCMOS12	1.108	0.551
LVCMOS15	1.109	0.043
LVCMOS25	1.110	0.044

When we use 28nm FPGA, there are 50.2%, 96.1% and 96.03% fall in total power dissipation using 23.3ºC Ambient Temperature for multiplier using LVCMOS12, LVCMOS15 and LVCMOS25 IO Standard respectively as shown in Table 3 and Figure 7.

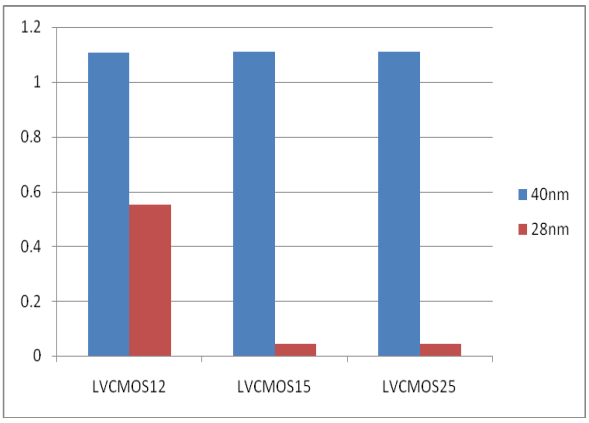

Figure 7: Total Power Dissipation on 23.3ºC Ambient Temperature

IV. CONCLUSION

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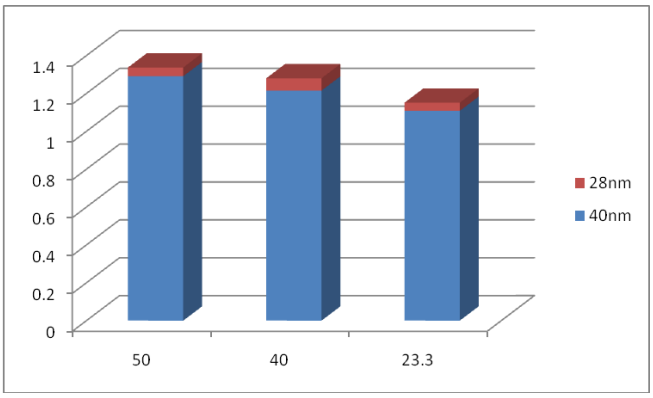

Figure 8: Comparison between 28nm and 40nm

The comparison graph between the power of different technologies 28nm and 40nm is shown in Figure 8. A decline in leakage power has been observed with decline in technology. In this project we have observed approx 87-88% decrease in leakage power dissipation when we shift from 40nm to 28nm technology based FPGA. Using 28nm technology on 23.3 ^{o}C and LVCMOS15 power efficiency has been achieved.

IV. FUTURE SCOPE

This energy efficient Vedic multiplier has reach to be implemented in digital signal processor also. We can amalgamate this multiplier with other arithmetic circuits and can design Vedic Processor or Vedic math co-processor. This design is implemented on 28nm 7-series and 40nm 6-series FPGA. There is wide scope to implement this design on ultra-scale FPGA. Here, the project is done by using LVCMOS I/O standard; also there is a wide scope to utilize I/O standards like GTL, SSTL, GTLP, HSTL and LVDCI

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