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HSTL Based Energy Efficient Vedic Multiplier Design on 28 nm FPGA Using Vedic Formula Adyamadyenantya

Arushi Aggarwal
Dept of ECE, Chitkara University, Chandigarh, India
missarohi4@gmail.com

Abstract: In this paper we have designed energy efficient Vedic multiplier circuit with units of inch or sq. ft. using family of various HSTL (High Speed Transreciever Logic) IO standards on 28 nm FPGA(Field programmable gate array).5 various HSTL standards are compared with each other to have the most efficient among them, there analysis is made on the basis of different temperatures taken : 25^0C, 30^0C, 45^0C, 53.5^0C.We are using Verilog HDL for the designing of this Vedic circuit.

Keywords: HSTL, Energy efficient, Vedic multiplier, 28nm FPGA.

I. INTRODUCTION

Vedic mathematics is a haul out as of four Vedas: books of wisdom. It is in fact a subordinate element of “Sthapatya-veda” (book about architecture and civil engineering). Due to its straight forwardness and promptness, it finds its great applications in the fields of geometry, trigonometry, factorization, multiplication and calculus. Multipliers are the important mechanisms for all the digital signal processors (DSPs), FIR filters etc. and the recital of these processors is mostly obtained by the types of multipliers being used. A number of multipliers have been projected and intended over past few years [1]. In those design , the multiplication method used requires many halfway stages to obtain the final output result because of which significant path gets prolonged.Also because of these prolonged paths additional hardware components are required leading to increase in power and area consumption .The technique used in this paper for multiplier design is named as **Adyamadyenantya – mantyena**
This sutra implies "first by first and last by last".
If assume we have to want to calculate the area of a rectangular plank having
length and breadth as 4ft . 2 inches and 5 ft. 7 inches respectively. Then in accordance with this sutra the area of this plank can be found as follows:

4’ 2"

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5’ 7"

4’ X 5’ = 20 sq. ft. i.e. First by first

2" X 7" = 14 sq. in. i.e. Last by last

and finally cross wise 4 X 7 + 5 x 2 = 28 +10 = 38.

regulate as many '12' s as likely towards left as 'units' => 38 = 3x12+2 , 3-:12's as 3 square feet make the first 20+3 = 23 sq. ft ; 2 left becomes 2x12 square inches and go towards right i.e. 2 x 12 = 24 sq. in. towards right gives 24+14 = 38 sq.in.

Thus we got the area in a quantity of 35 sq uints and another quantity of 128 sq. units.

i.e. 35 sq. ft 128 sq. in. We are implementing the design on 28 nm FPGA and 5 different IO standards of HSTL family to find the most energy efficient among them. In order to analyse how an electric device works on varying the temperature of the surrounding in which it is placed, we have chosen different temperatures.

II. Maximum Ambient, Junction Temperature and Leakage Power

A. Analysis of MAT, Junction temperature and Leakage power for various IO standards

Table 1: Analysis of Leakage Power, Total power dissipation, JT for HSTL_1

	Leakage Power	Total Power	Junction Temperature
25	0.045	0.292	25.6
40	0.066	0.313	40.6
53.5	0.100	0.347	54.2
60	0.125	0.371	60.8

There is 64%, 21.29%, 57.89% reduction in Leakage power, Power Dissipation and JT temperature in that order when the ambient temperature is range down from 25^0C to 60^0C for SSTL_1 IO standard.

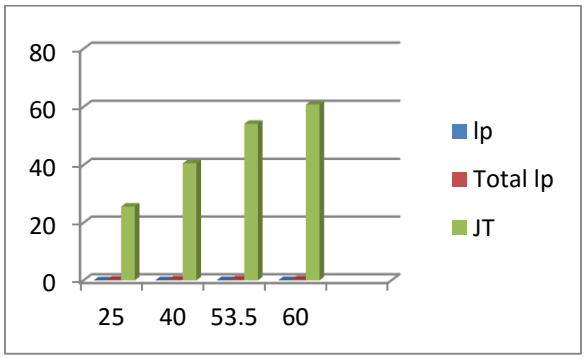

Figure 1: Graphical representation of LP, Total Dissipation power, JT FOR HSTL_1

Table 2: Analysis of Leakage Power, Total power dissipation, JT for HSTL_11

	Leakage Power	Total Power	Junction Temperature
25	0.045	0.290	25.6

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40	0.066	0.311	40.6
53.5	0.100	0.345	54.2
60	0.125	0.370	60.8

There is 64%, 21.62%,57.89% reduction in power, Power Dissipation and JT temperature in that order when the ambient temperature is range down from 25^0C to 60^0C for SSTL_11 IO standard.

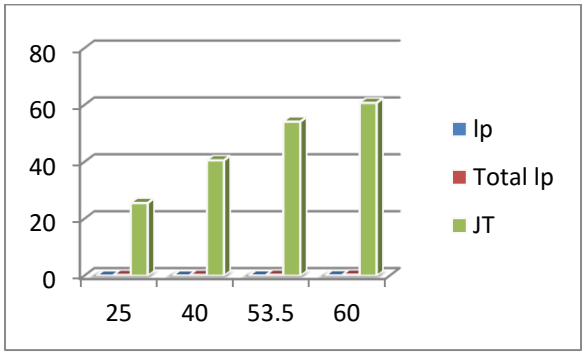

Figure 2: Graphical representation of LP,Total Dissipation power,JT For HSTL_11

Table 3: Analysis of Leakage Power, Total power dissipation, JT for HSTL_1_DCI

	Leakage Power	Total Power	Junction Temperature
25	0.047	1.047	27.1
40	0.069	1.069	42.2
53.5	0.105	1.106	55.8
60	0.132	1.132	62.3

There is 64.39%, 7.50%,56.50% reduction in power, Power Dissipation and JT temperature temperature in that order when the ambient temperature is range down from 25^0C to 60^0C for SSTL_11_DCI IO standard.

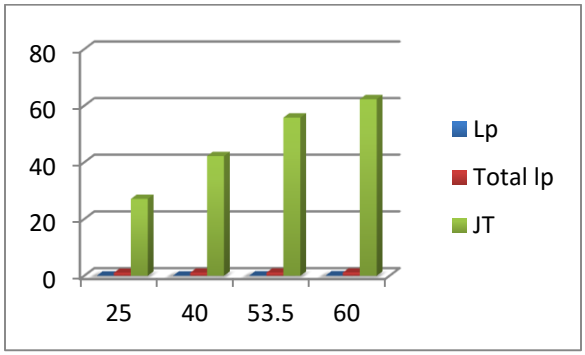

Figure 3Graphical representation of LP,Total Dissipation power,JT For HSTL_11_DCI

Table 4: Analysis of Leakage Power, Total power dissipation, JT for HSTL_11_DCI

	Leakage Power	Total Power	Junction Temperature

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25	0.047	0.897	26.8
40	0.068	0.919	41.9
53.5	0.104	0.955	55.5
60	0.130	0.981	62.0

There is 63.84%, 8.56%,56.77% reduction in power, Power Dissipation and JT in that order when the ambient temperature is range down from 25^0C to 60^0C for SSTL_1_DCI IO standard.

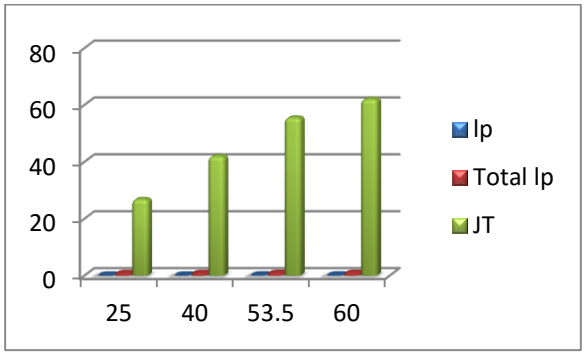

Figure 4Graphical representation of LP, Total Dissipation power,JT For HSTL_1_DCI

III. LEAKAGE POWER

Table 5: Leakage Power analysis for various IO standards

	25^0C	40^0C	53.5^0 C	60^0C
HSTL_1	0.045	0.066	0.100	0.125
HSTL_11	0.045	0.066	0.100	0.125
HSTL_1_DCI	0.047	0.068	0.104	0.130
HSTL_11_DCI	0.047	0.069	0.105	0.132

At different ambient temperatures from 25º C to 60º C, there is 4.44%, 4.34%, 4.76%, 5.303% reduction in Leakage power for HSTL_11 as compared to HSTL_11, HSTL_11_DCI, HSTL_11_DCI

IV. TOTAL POWER DISSIPATION

Table 6: Total Power Dissipation analysis for various IO standards

	25^0C	40^0C	53.5^0C	60^0C
HSTL_1	0.292	0.313	0.347	0.371
HSTL_11	0.290	0.311	0.345	0.370
HSTL_1_DCI	0.897	0.919	0.955	0.981
HSTL_11_DCI	1.047	1.069	1.106	1.132

At different ambient temperatures from 25º C to 60º C, there is 72.30%, 70.90%, 68.80%, 67.31% reduction in Total power Dissipation for HSTL_11 as compared to HSTL_11, HSTL_11_DCI, HSTL_11_DCI.

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JUNCTION TEMPERATURE

Table 7:Junction Temperature analysis for various IO standards

	25^0C	40^0C	53.5^0 C	60^0C
HSTL_1	25.6	40.6	54.2	60.8
HSTL_11	25.6	40.6	54.2	60.8
HSTL_1_DCI	26.8	41.9	55.5	62.0
HSTL_11_DCI	27.1	42.2	55.8	62.3

At different ambient temperatures from 25^o C to 60^o C, there is 5.35%, 3.79%, 2.86%, 2.40% reduction in Junction Temperature for HSTL_11 as compared to HSTL_11, HSTL_11_DCI, HSTL_11_DCI.

V. CONCLUSION

The design of energy efficient Vedic multiplier by the sutra Adyamadyenantya – mantyena is possible and we concluded that the design based on the IO standard of HSTL_11 member of HSTL family is the most energy efficient design. From the analysis done above we observed that At different ambient temperatures from 25^o C to 60^o C, there is 4.44%, 4.34%, 4.76%, 5.303% reduction in Leakage power and 72.30%, 70.90%, 68.80%, 67.31% reduction in Total power Dissipation for HSTL_11 as compared to HSTL_11, HSTL_11_DCI, HSTL_11_DCI.

VI. FUTURE SCOPE

The design is implemented on 28 nm FPGA. Hence, there is a broad extent to execute this design on 45 nm Spartan-6, Artix-6 and Virtex-5 FPGA or on 42nm, 10nm, 5nm or 7 nm based Field programmable gate array in future. The design on these technologies will give a wide scale for VLSI designer to obtain highly energy efficient and high performance multiplier design. This design can be applied to various electronic circuits such as processors, ALU's, registers etc. in order to manage leakage power.

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