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Capacitance Scaling Based Energy Efficient Vedic Divider using Paravartya Yojayet on 28nm FGPA

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Abstract-In this paper, we have designed an energy efficient Vedic Divider using an ancient Vedic mathematics technique known as "ParavartyaYojayet". ParavartyaYojayet is a Sanskrit name which means transpose and adjust. Vedic mathematical formulas are used to solve tedious and cumbersome arithmetic operations. Today's world demands implementation of techniques which take lesser time and are energy efficient so we have designed a Vedic divider to solve long divisions in seconds. Our design consists of 2 inputs for dividend and divisor and 2 outputs that are remainder and quotient. Many researchers have done research work on Vedic mathematics to solve DSP operations using Urdhava-Triyagbhayam multiplication sutra, to design asynchronous Vedic DSP processor core and lots more. In our paper we have implemented our code on Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform. We have done power analysis by varying frequencies and capacitance to make our Vedic divider energy efficient. Analysis results that the maximum power is consumed at 2.2GHz and minimum power is consumed at 1.2GHz. In respect of capacitance maximum power is consumed at 100pF and minimum power is consumed at 20pF.

Keywords. Paravartyayojayet, Vedic mathematics, FGPA, Energy Efficient, Vedic Divider

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1 Introduction

Ancient mathematics is known as Vedic mathematics [1-2]. Vedic mathematics is part of four Vedas (books of wisdom)[3].Vedic mathematics deals with various Vedic mathematical formulae and their applications to carry out tedious and cumbersome arithmetic operations[4].the Vedic mathematics sutra are from Vedas that were used by our ancient scholars to make mathematical calculations faster, when there were no calculators and computers[5]. This Vedic mathematics can be used to solve algebra easily [5]. Figure 1 represents the division of sutras. Sutras can be used for arithmetic computation and also for algebra computation. Figure 2 shows the list of 18 sutras. These sutras cover all fields of mathematics geometry, arithmetic etc. research is been carried out in many areas. With the help of these sutras we can easily solve the complex calculations. These sutras are very helpful in solving calculus, geometry problems. Application of Vedic sutras spares a lot of time and effort in solving problems.

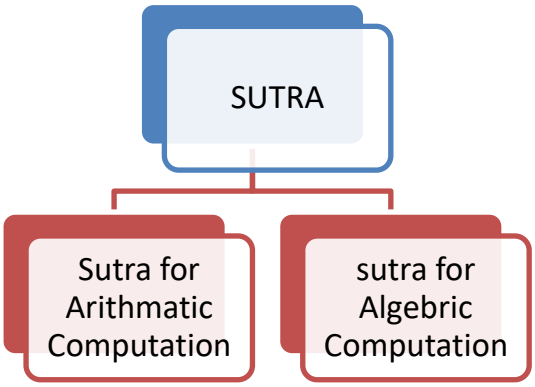

Fig. 1. Types of Sutra (Formula) in Vedic Mathematics

Many papers have been published using Vedic mathematics for different applications. A paper was published which includes DSP operations based on ancient Vedic mathematics using Vedic Urdhava-Triyagbhayam multiplication sutra [6]. A design of an 8 bit fixed point, asynchronous Vedic DSP processor core has also been studied [7]. Today's world demands implementation of techniques which take lesser time and is energy efficient so we have designed a Vedic divider. other researchers have also performed there research work in the field of Vedic mathematics like implementation of 4*4 multiplier using Urdhva-Tiryakbhyam in 45nm technology[8], another division architecture using another Vedic technique known as `Dhwajam'[9]. With the enrichment of new technology there is a huge demand of energy efficiency. Keeping this in our mind we have designed a Vedic divider which is energy efficient and we have tested in

on 28nm FGPA family Kintex-7. Power analysis has been done to make it energy efficient by varying values of capacitance and frequencies.

1. •Ekadhikena Purvena
2. •Nikhilam navatascaramam Dasatah
3. •Urdhva - tiryagbhyam
4. •**Paravartya Yojayet**
5. •Sunyam Samya Samuccaye
6. •Anurupye - Sunyamanyat
7. •Sankalana - Vyavakalanabhyam
8. •Puranapuranabhyam
9. •Calana - Kalanabhyam
10. •Ekanyunena Purvena
11. •Anurupyena
12. •Adyamadyenantya - mantyena
13. •Yavadunam Tavadunikrtya Varganca Yojayet
14. •Antyayor Dasakepi
15. •Antyayoreva
16. •Lopana Sthapanabhyam
17. •Vilokanam
18. •Gunita Samuccayah

Fig. 2. List of Vedic Formula (Sutra) in Vedic Mathematics

LVCMOS IO standard is used to design FPGA based Thermal Aware Energy Efficient Vedic Multiplier based on Urdhva Tiryagbhyam [10]. In order to achieve speed and high performance in addition to energy efficiency, HSTL IO standard is also used along with LVCMOS for design of energy efficient Vedic multiplier based on Urdhva Tiryagbhyam [11]. Capacitance scaling is one of the best energy efficient technique for FPGA based VLSI design. Earlier capacitance scaling is also used to design of energy efficient ROM [12], energy efficient UART [13] and power optimized register [14]. Here we are going to utilize the benefit of capacitance scaling for this Vedic Divider based on Vedic formula of Parvartya Yojayet.

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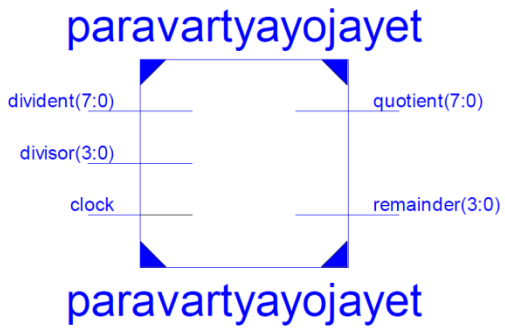

Fig. 3. Top Level Schematic of ParavartyaYojayet Sutra Based Vedic Divider

This Vedic divider has three inputs and two outputs as shown in Figure 3. One input is clock pulse. Second input is 8-bit dividend. Third input is 4-bit divisor. First output is 8-bit quotient and second output is 4-bit remainder. For example, if dividend is 254 (8'b11111110) and divisor is 12(4'b1100) then quotient is 21(8'b00010101) and remainder is 2 (4'b0010). Our paper deals with ParavartyaYojayet, this is a Sanskrit name meaning transpose and adjust. In this work a Vedic divider is designed using ParavartyaYojayet. The code has been implemented in Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform. All our work is done on 28nm FPGA kintex-7. ParvartyaYojayet algorithm is implemented to develop a high performance divider and static timing analysis is also done on Vedic divider [3]. In this paper, we have tried to make an energy efficient ParvartyaYojayet Vedic divider with 2 inputs and 2 outputs.

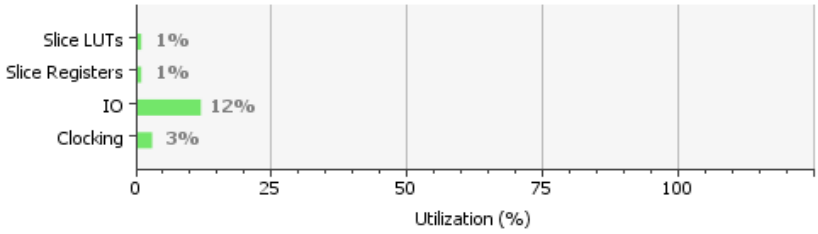

Fig. 4. FPGA Resource Utilization by Paravartya Yojayet Based Vedic Divider

This design is using only 1% Slice LUTs, 1% Slice Registers, 12% IO and 3% clocking available on Kintex-7 FPGA.

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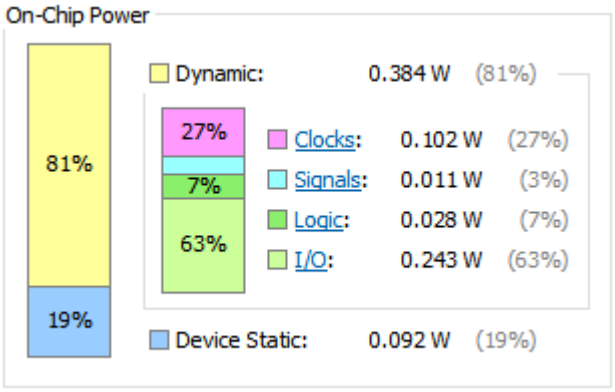

Fig. 5. On-Chip Power Dissipation of Our Design on Kintex-7 FPGA

When we are doing on-chip power analysis of Vedic divider on Kintex-7 FPGA, then this design is using 19% Static power and 81% dynamic power. Out of 81% dynamic power, 27% is clock power, 3% is signals power, 7% is logic power and 63% IO power.

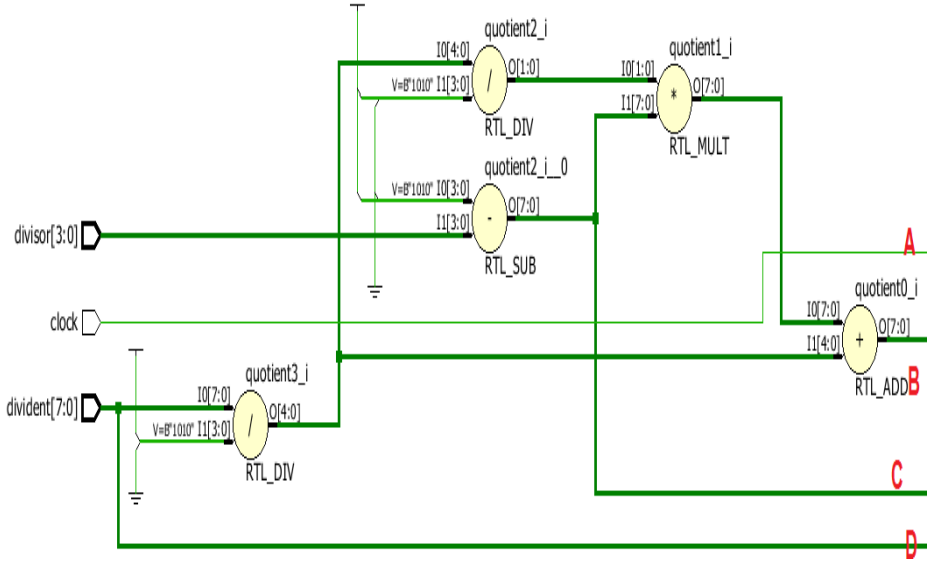

Fig. 6. RTL Schematic of Parvartya Yojayet: Part I

Step 1: Divide 254 by 12.

Step 2: We separate last digit 4 (i.e. 254%10) from dividend 254 for remainder and 25 (i.e. 254/10) for later division process as shown in Figure 6.

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Step 3: We minus divisor 12 from 10 and get -2. Multiply this -2 by first digit of 25 i.e.2 and we finally get -4 and add -4 to 25 and get 21 as quotient as shown in Figure 6.

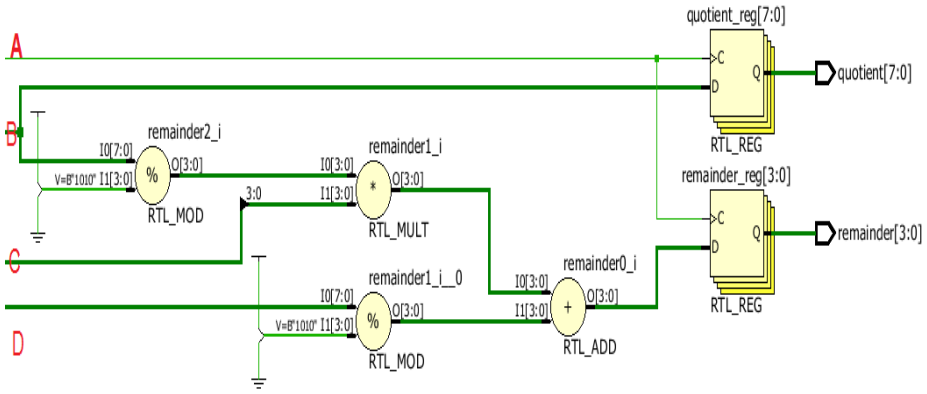

Fig. 7. RTL Schematic of Parvartya Yojayet: Part II

Step 4: Take Mod of 21 and 10 and multiply 1 (i.e.21%10) with -2 and add final result -2 in remainder 4 (in step 1) and final remainder is 2 as shown in Figure 7.

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2 Power Analysis of Vedic Divider on Kintex-7 FPGA

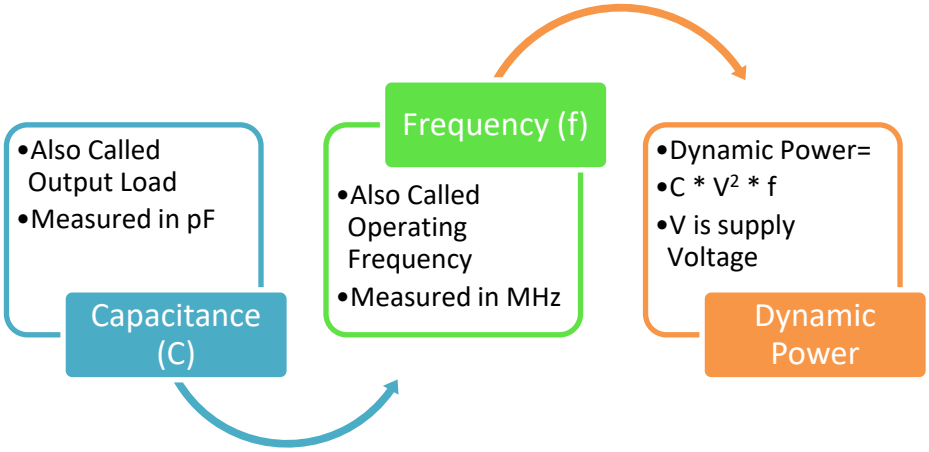

Fig. 8. Role of Capacitance and Frequency in Dynamic Power Dissipation

Dynamic power is directly proportional to capacitance and frequency as shown in Fig.8. When we scale down capacitance, power dissipation will decrease in same proportion. Ambient temperature is constant 25 degree Celsius. Airflow is 250 LFM. LFM is Linear Feet per Minute. Unit of capacitance is pico Farad (pF).

2.1 Power Analysis of Vedic Divider for 1400 MHz Operating Frequency

Table 1. Power Analysis at 25°Celsius Ambient Temperature and 250 LFM Airflow

Capacitance in pF	Total Power
20pF	1.567
40pF	2.470
60pF	3.373
80pF	4.276
100pF	5.179

There is 69.74% reduction in total power dissipation when we use 28nm FPGA and capacitance is scaled down from 100pF to 20pF as shown in Table 1 and Fig. 9. Here,

device operating frequency is constant 1400MHz. So, power is changing with change in capacitance.

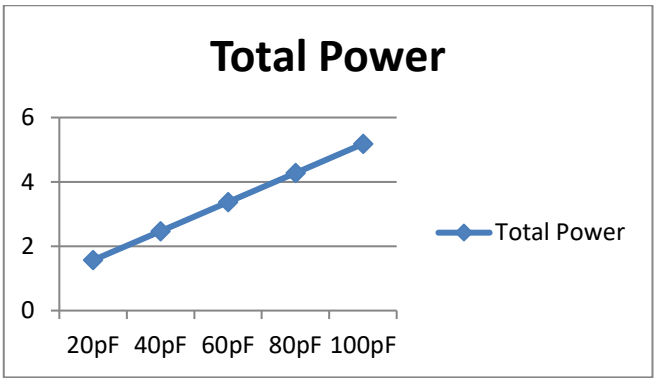

Fig. 9. Power Dissipation at 25ºCelsius Temperature and 1400MHz Frequency

2.2 Power Analysis for 1.2 GHz Device Operating Frequency

Here, device operating frequency is constant 1200MHz, airflow is also constant 250 LFM, and ambient temperature is also constant 25 degree Celsius. So, power is decreasing with decrease in capacitance. Unit of power is Watt (W) and unit of Capacitance is pico Farad (pF). Pico is unit that is 10^{-12} in magnitude.

Table 2. Power Analysis at 25ºCelsius Ambient Temperature and 250 LFM Airflow

Capacitance in pF	Total Power
20pF	1.317
40pF	2.068
60pF	2.819
80pF	3.570
100pF	4.322

There is 69.52% reduction in total power dissipation when we use 28nm FPGA and capacitance is scaled down from 100pF to 20pF as shown in Table 2 and Fig.10.

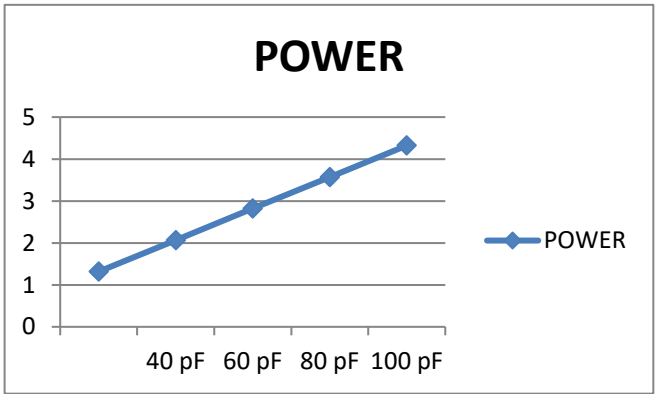

Fig. 10. Power Dissipation at 25ºCelsius Temperature and 1.2GHz Frequency

2.3 Power Analysis for 2100 MHz Device Operating Frequency

Here, device operating frequency is constant 2100MHz, airflow is also constant 250 LFM, and ambient temperature is also constant 25 degree Celsius. So, power is decreasing with decrease in capacitance. Unit of power is Watt (W) and unit of Capacitance is pico Farad (pF). Pico is unit that is 10^{-12} in magnitude.

Table 3. Power Analysis at 25ºCelsius Ambient Temperature and 250 LFM Airflow

Capacitance in pF	Total Power
20pF	2.414
40pF	3.830
60pF	5.248
80pF	6.666
100pF	8.085

There is 70.14% reduction in total power dissipation when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 3 and Fig.11.

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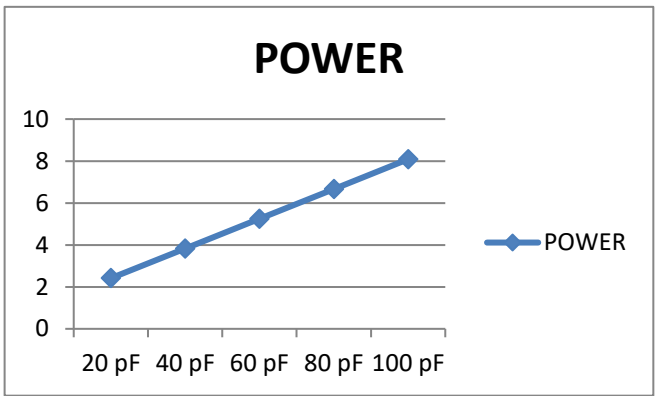

Fig. 11. Power Dissipation at 25ºCelsius Temperature and 2100MHz Frequency

2.4 IO Power Analysis for 1700 MHz Device Operating Frequency

Here, device operating frequency is constant 1700MHz, airflow is also constant 250 LFM, and ambient temperature is also constant 25 degree Celsius. So, power is decreasing with decrease in capacitance. Unit of power is Watt (W) and unit of Capacitance is pico Farad (pF). Pico is unit that is 10^{-12} in magnitude.

Table 4. Power Analysis at 25ºCelsius Ambient Temperature and 250 LFM Airflow

Capacitance in pF	Total Power
20pF	1.922
40pF	3.040
60pF	4.426
80pF	5.618
100pF	6.810

There is 71.77% reduction in total power dissipation when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 4 and Fig.12.

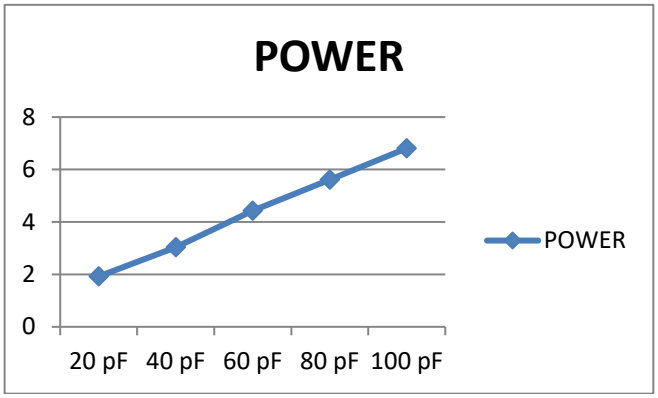

Fig. 12. Power Dissipation at 25ºCelsius Temperature and 1700MHz Frequency

2.5 Power Analysis for 1800 MHz Device Operating Frequency

Here, device operating frequency is constant 1800MHz, airflow is also constant 250 LFM, and ambient temperature is also constant 25 degree Celsius. So, power is decreasing with decrease in output load. Unit of power is Watt (W) and unit of Capacitance is pico Farad (pF). Pico is unit that is 10^{-12} in magnitude. Capacitance is also called output load.

Table 5. Power Analysis at 25ºCelsius Ambient Temperature and 250 LFM Airflow

Capacitance in pF	Total Power
20pF	2.043
40pF	3.234
60pF	4.426
80pF	5.618
100pF	6.810

There is 70% reduction in total power dissipation when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 6 and Fig.14.

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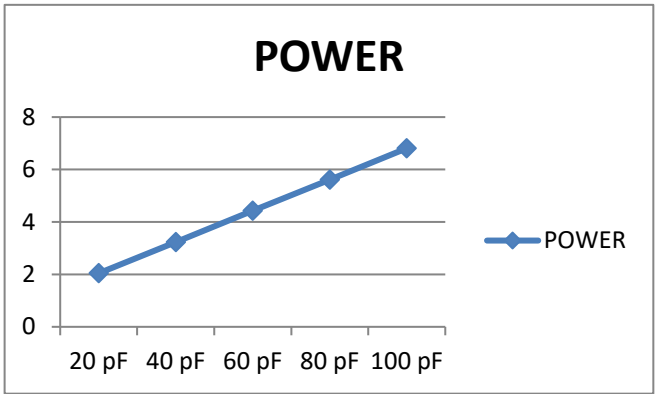

Fig. 13. Power Dissipation at 25ºCelsius Temperature for 1800MHz Frequency

2.6 Power Analysis for 2.2 GHz Device Operating Frequency

Here, device operating frequency is constant 2200MHz, airflow is also constant 250 LFM, and outside environment temperature is 25 degree Celsius. Therefore, power is increasing with increase in capacitance. Unit of power is Watt (W) and unit of Capacitance is pico Farad (pF). Pico is unit that is 10^{-12} in magnitude.

Table 6. Power Analysis at 25ºCelsius Ambient Temperature and 250 LFM Airflow

Capacitance in pF	Total Power
20pF	2.541W
40pF	4.034W
60pF	5.528W
80pF	7.023W
100pF	8.519W

There is 70.17% reduction in total power dissipation when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 6 and Fig.14.

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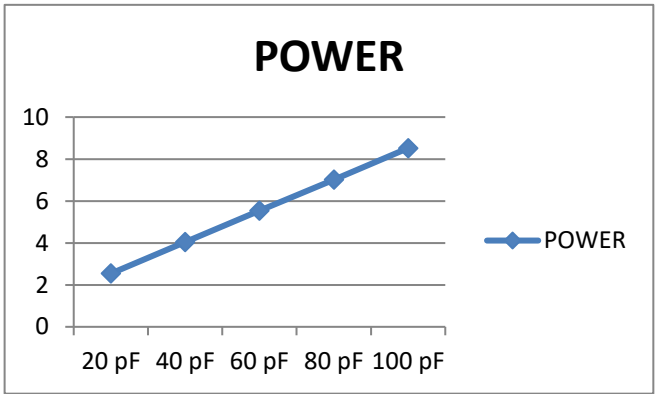

Fig. 14. Power Dissipation at 25ºCelsius Temperature for 2.2GHz Frequency

2.7 Power Analysis for Different Frequencies at Different Capacitance

Table 7. Power Dissipation of Vedic Divider at 25ºC Temperature, and 250 LFM Airflow

Frequency	20 pF	40 pF	60 pF	80 pF	100 pF
1400MHz	1.567	2.470	3.373	4.276	5.179
1.2GHz	1.317	2.068	2.819	3.570	4.322
2100MHz	2.414	3.830	5.248	6.666	8.085
1700MHz	1.922	3.040	4.426	5.618	6.810
1800MHz	2.043	3.234	4.426	5.618	6.810
2.2GHz	2.541	4.034	5.528	7.023	8.519

Table 7 and Fig.15 tells us that the maximum power is consumed at 2.2GHz and minimum power is consumed at 1.2GHz. In respect of capacitance maximum power is consumed at 100pF and minimum power is consumed at 20pF.

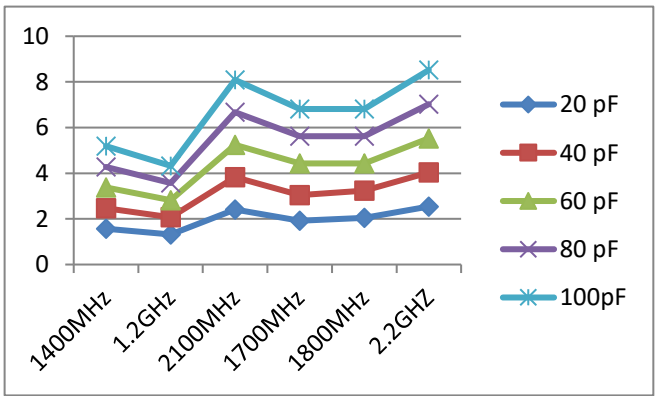

Fig. 15. Power Dissipation at 25ºCelsius Temperature for Different Frequencies and Capacitances

3 Conclusion

The design is energy efficient and the code has been implemented in Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform. This Vedic divider consists of 2 inputs that are dividend and divisor and 2 outputs that are remainder and quotient. The design is tested by varying capacitance at different frequencies keeping the temperature constant that is 25 degree Celsius. We can conclude from this design that the maximum power is consumed at 2.2GHz and minimum power is consumed at 1.2GHz. In respect of capacitance maximum power is consumed at 100pF and minimum power is consumed at 20pF.

4 Future Scope

The future scope of Capacitance Scaling Based Energy Efficient Vedic divider using ParavartyaYojayet on 28nm FGPA is that we have used 28nm FGPA that is Kintex-7. We can also implement this design on 22nm or 18 nm FGPA. We can also use different FGPA families like automotive Artix7, automotive Coolrunner2, automotive Spartan, automotive Spartan-3A DSP, automotive Spartan 3A, automotive Spartan 3E, automotive Spartan6, Spartan3, Spartan3E.Here, we are using capacitance scaling techniques. We can redesign this Vedic divider with other energy efficient technique like frequency scaling, thermal scaling, clock gating, and impedance matching with different logic family, and mapping. We can also change values of frequencies and can change the range of capacitance.

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