Gyancity Journal of Engineering and Technology,
Vol.2, No.1, pp. 62-69, January 2016
ISSN: 2456-0065 DOI: 10.21058/gjet.2016.2107

Clock Gating Based Low Power Energy Efficient Gurmukhi Unicode Reader Design on FPGA

Sunny Singh, Amanpreet Kaur
School of Computer Sciences
Chitkara University,
Rajpura, India
Er.singhsunny2207@gmail.com

***Abstract*— In the domain of High Performance Energy Efficient Computing (HPEEC), the focus of research is shifting toward energy efficient computing or low power VLSI design or green computing. We are applying three different clock gating technique in target design of Gurmukhi Unicode Reader (GUR). These power saving techniques reduce the power dissipation of GUR in significant amount. It has been observed that if we switch to flip flop based clock gating instead of simple clock then we can save 89.6% of clock power and we can save 90.48% of clock power if we switch to latch free clock gating (LFCG) or latch based clock gating (LBCG) in case of all SSTL based logic families. It has been observed that if we switch to flip flop based clock gating instead of simple clock then we can save 23.88% of IO power and we can save 26.59% of IO power if we switch to either LFCG or LBCG in case of SSTL2_II_DCI. It has been observed that if we switch to FFBCG instead of simple clock then we can save 52.38% of total power and we can save 56.67% of total power if we switch to either LFCG or LBCG in case of SSTL2_II_DCI.**

***Index Terms*— Low Power, Energy Efficient, Gurmukhi Unicode, FPGA, SSTL.**

1. Introduction

Clock gating is an energy efficient technique. It is used for power savings by gating off the functional units not required by the currently executing instruction, as determined by the Instruction Decoder unit [1].

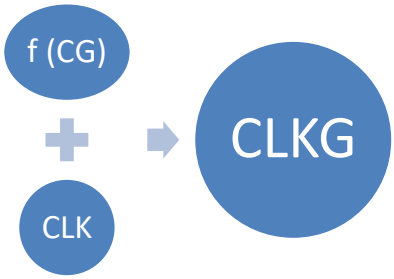

Figure 1: Principles of Clock Gating

When the idle condition is true, the clock signal is calculated by function f (CG) as shown in Figure 1. CLK is the system clock and CLKG is the gated clock of the functional unit. According to reference [1], Power optimization traditionally relegated to the synthesis and circuits level, now shifted to the System Level and Register-Transfer-Level. This is possible due to clock gating which switch off the inactive units of the design and reduce overall power consumption. There are many clock gating styles in [1] available to optimize power in VLSI circuits [2].

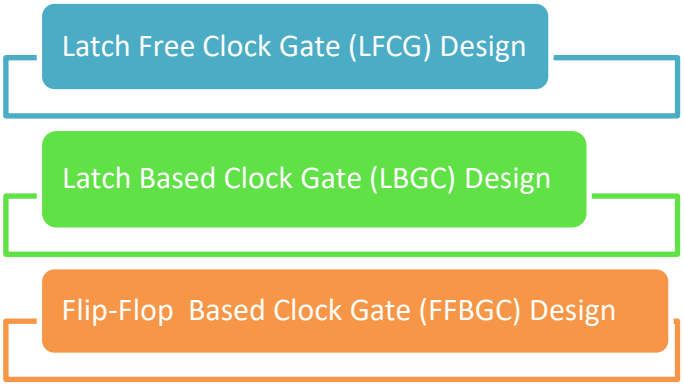

Figure 2: Different Clock Gating Styles

As shown in Figure 2, there are three clock gating styles. These are Latch Free Clock Gating, Latch Based Clock Gating, Flip-Flop Based Clock Gating. Stub Series Terminated Logic (SSTL) is a group of electrical standards for driving transmission lines commonly used with DRAM based DDR memory IC's and memory modules. The Stub-Series Terminated Logic (SSTL) for 2.5V (SSTL2) and 1.8V (SSTL18) standards are for general purpose memory buses.Virtex-6 FPGA I/O supports both standards for single-ended signaling and differential signaling. This standard requires a differential amplifier input buffer and push-pull output buffer. For energy efficient design, we generally use IO standards. HSTL [8] and LVCMOS I/O standard [6-7] are used for energy efficient design. We are extending our work to SSTL IO standards with combination of clock gating [1, 2,5]. SSTL18_II, SSTL15, SSTL2_II_DCI, SSTL18_II_DCI, SSTL2_II, SSTL15_DCI are six different IO Standards available on FPGA as shown in Figure 3. We are using these 6 different IO for energy efficient Gurmukhi Unicode reader design along with clock gating.

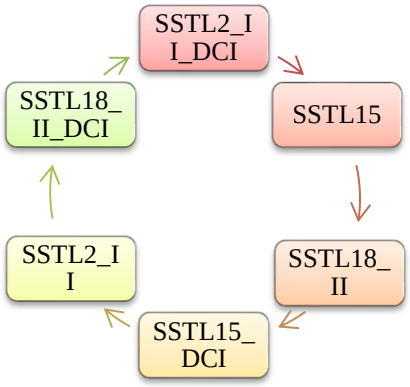

Figure 3: Different SSTL IO Standards

2. Gurmukhi Unicoder

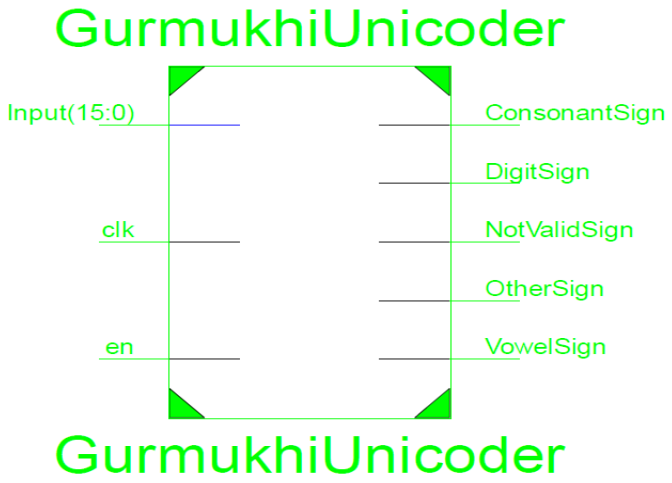

Figure 4: RTL Schematic of Gurmukhi Unicoder

The word Gurumukhi means "from the Guru's mouth" [3] and Shahmukhi translating into "from the King's mouth" [4]. This energy efficient Unicode reader design [5-6] deals with hardware aspects of natural language processing. Table 1 shows the representation of vowels used in Gurmukhi in the hexadecimal form. Similarly, we have hexadecimal codes for consonants, digits and other signs in Gurmukhi.

Table1: Unicodes for various vowels used in Gurmukhi

VARIOUS VOWELS USED IN GURMUKHI	
0A05 ਅ	GURMUKHI LETTER A
0A06 ਆ	GURMUKHI VOWEL SIGN AA
0A07 ਇ	GURMUKHI LETTER I
0A08 ਈ	GURMUKHI LETTER II
0A09 ਉ	GURMUKHI LETTER U
0A0A ਊ	GURMUKHI LETTER UU
0A0F ਏ	GURMUKHI LETTER EE
0A10 ਐ	GURMUKHI LETTER AI
0A13 ਓ	GURMUKHI LETTER OO
0A14 ਔ	GURMUKHI LETTER AU
0A40 $ੀ	GURMUKHI VOWEL SIGN II
0A40 $ੀ	GURMUKHI VOWEL SIGN II
0A41 $ੁ	GURMUKHI VOWEL SIGN U
0A42 $ੂ	GURMUKHI VOWEL SIGN UU
0A47 $ੇ	GURMUKHI VOWEL SIGN EE
0A48 $ੈ	GURMUKHI VOWEL SIGN AI
0A4B $ੋ	GURMUKHI VOWEL SIGN OO
0A4C $ੌ	GURMUKHI VOWEL SIGN AU

ISSN: 2456-0065 DOI: 10.21058/gjet.2016.2107

0A05 ਅ	GURMUKHI LETTER A
0A06 ਆ	GURMUKHI LETTER AA
0A07 ਇ	GURMUKHI LETTER I
0A08 ਈ	GURMUKHI LETTER II
0A0A ਉ	GURMUKHI LETTER UU
0A0F ਏ	GURMUKHI LETTER EE
0A10 ਐ	GURMUKHI LETTER AI
0A13 ਓ	GURMUKHI LETTER OO
0A14 ਔ	GURMUKHI LETTER AU

3. Clock Gating

1. Latch-Free Based Clock Gating Design

For active high logic, we are using AND gate. For active low logic, we use OR gate to form clock gate without using latch.

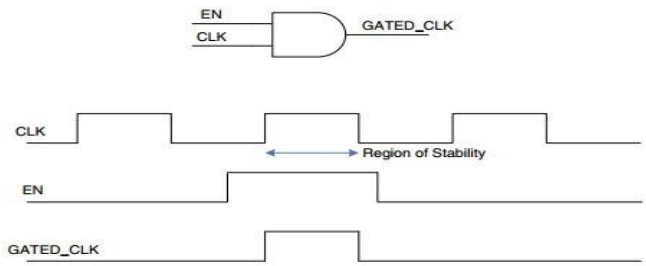

Figure 5: Latch-Free Based Clock Gating Design

In LFCG, Enable (EN) and Clock (CLK) are two inputs and GATED_CLK is output. We have to hold enable signal high for at least duration of clock period in order to avoid glitches as shown in Figure 4.

2. Latch-Based Clock Gating Design

LBCG has a level sensitive latch in order to hold the enable signal during entire clock period. There are two types of LBCG design. OR gate is used with latch when clock is low. Combination of latch with AND gate when clock is high as shown in Figure 5.

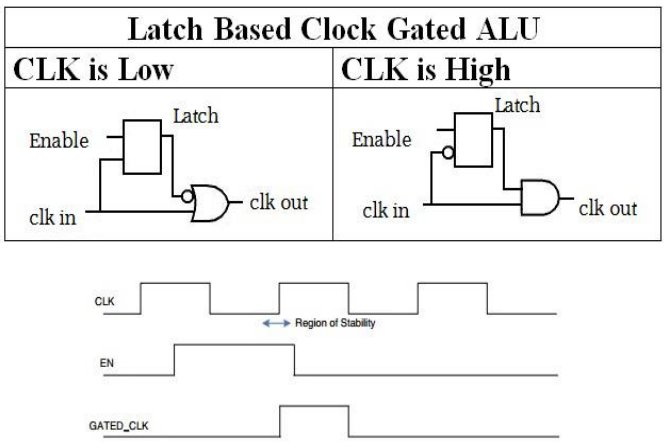

Figure 6: Latch-Based Clock Gating Design [2]

Latch based design is not testable. Therefore, we are using flip-flop based clock gating.

3. Flip Flop Based Clock Gating Design
In one FBCG, flip-flop with OR gate is in use when clock is low. In other FBCS, AND gate is used with flip-flop when clock is high as shown in Figure 6.

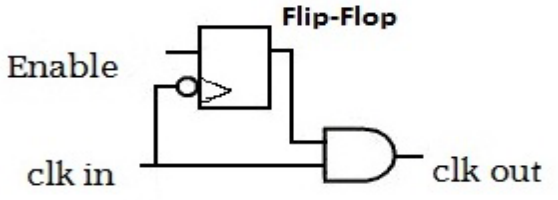

Figure 7: Flip Flop Based Clock Gating Design [2]

4. Results

There is significant reduction in clock power but only a minor reduction in IOs power possible with clock gating. For further reduction in IOs power, we use IO standard technique. IO standard is a matching of impedance of transmission line and input/output port. In this paper we have observed the clock power, IO power and total power at SSTL IO standard. All the three powers are being analyzed at different standards of SSTL based logic families. In the following table clock power has been at different SSTL based IO standards.

Table 2: Clock Power Measurement of Gurmukhi Unicoder

CLOCK POWER OF DIFFERENT SSTL LOGIC FAMILIES AT A FREQUENCY OF 1 THz					
S.No.	Logic Family	W/o CG	LFCG	LBCG	FFBCG
1.	SSTL2_II	15.959	1.219	1.219	1.658
2.	SSTL18_II	15.959	1.219	1.219	1.658
3.	SSTL15	15.959	1.219	1.219	1.658
4.	SSTL2_II_DCI	15.959	1.219	1.219	1.658
5.	SSTL18_II_DCI	15.959	1.219	1.219	1.658
6.	SSTL15_DCI	15.959	1.219	1.219	1.658

It has been observed that if we switch to flip flop based clock gating instead of simple clock then we can save 89.6% of clock power and we can save 90.48% of clock power if we switch to latch free clock gating and latch based clock gating in case of all SSTL based logic families as shown in the Figure 8 and Table 2.

ISSN: 2456-0065 DOI: 10.21058/gjet.2016.2107

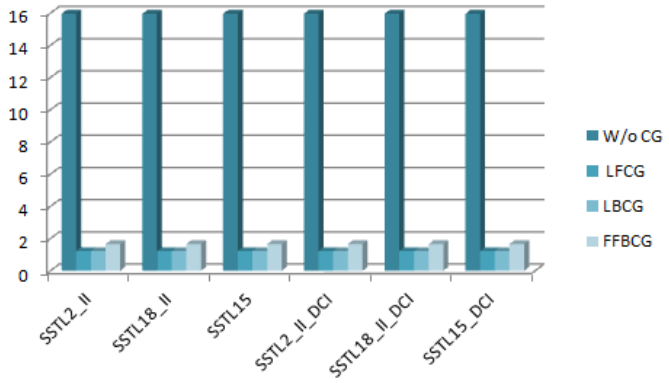

Figure 8: Clock Power Measurement with and without Clock Gating

In the following table the IO power has been analyzed at different SSTL based IO standards.

Table 3: IO Power Measurement of Gurmukhi Unicoder

IO POWER OF DIFFERENT SSTL LOGIC FAMILIES AT A FREQUENCY OF 1 THz					
S.No.	Logic Family	W/o CG	LFCG	LBCG	FFBCG
1.	SSTL2_II	22.446	18.517	18.517	18.814
2.	SSTL18_II	17.147	13.218	13.218	13.515
3.	SSTL15	15.911	11.982	11.982	12.279
4.	SSTL2_II_DCI	14.944	10.970	10.970	11.375
5.	SSTL18_II_DCI	15.235	11.284	11.284	11.635
6.	SSTL15_DCI	15.850	11.908	11.909	12.240

It has been observed that maximum power reduction occurs is in the case of SSTL2_II_DCI logic family in which if we operate the circuit with clock only then total power consumption is of 14.944Watts. But if switch to latch free or latch based clock gating instead of simple clock than there is a consumption of only 10.970 Watts which means there is 26.59% reduction in power and furthermore if we switch on to flip flop based clock gating then we can save 23.88% of power as shown in Figure 9 and Table 3.

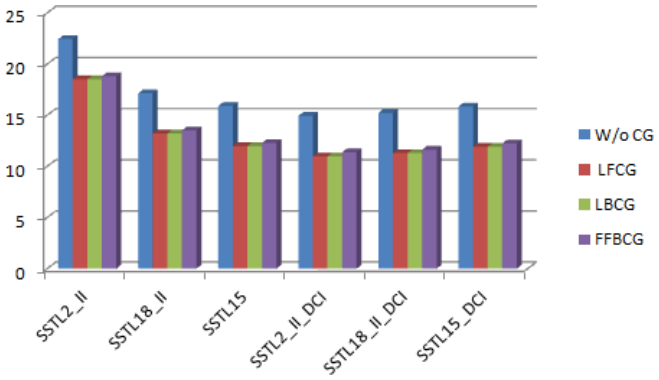

Figure 9: IO Power Measurement with and without CLOCK Gating

In the following table the total power has been analyzed at different SSTL based IO standards.

ISSN: 2456-0065 DOI: 10.21058/gjet.2016.2107

Table 4: Total Power Measurement of Gurmukhi Unicoder

TOTAL POWER OF DIFFERENT SSTL LOGIC FAMILIES AT A FREQUENCY OF 1 THz					
S.No.	Logic Family	W/o CG	LFCG	LBCG	FFBCG
1.	SSTL2_II	40.335	21.768	21.768	23.070
2.	SSTL18_II	35.035	16.469	16.468	17.770
3.	SSTL15	33.798	15.232	15.232	16.534
4.	SSTL2_II_DCI	32.833	14.221	14.221	15.630
5.	SSTL18_II_DCI	33.123	14.535	14.534	15.890
6.	SSTL15_DCI	33.737	15.160	15.159	16.495

It has been observed that maximum power reduction occurs is in the case of SSTL2_II_DCI logic family in which if we operate the circuit with clock only then total power consumption is of 32.833 Watts. But if switch to latch free or latch based clock gating instead of simple clock than there is a consumption of only 14.221 Watts which means there is 56.67% reduction in power and furthermore if we switch to flip-flop based clock gating then we can save 52.38% of power as shown in Figure 10 and Table 4.

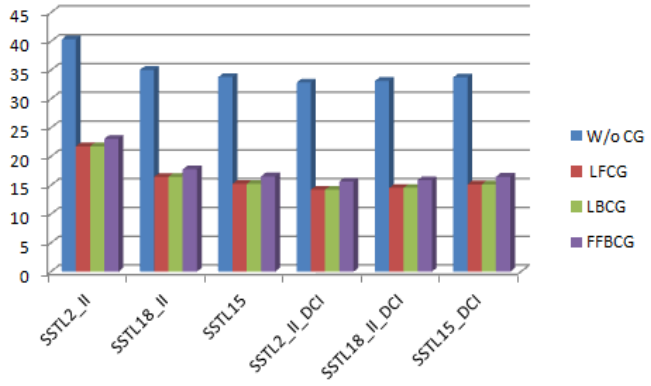

Figure 10: Total Power Measurement with and without Clock Gating

5. Conclusion

Clock gating is the most efficient technique to reduce clock power as well as dynamic power dissipation in compare to power dissipation without clock gating. Latch Free Clock gating technique is the most efficient clock gating technique in compare to Flip-Flop based clock gating. It has been concluded that as far as a clock power is being concerned then we can save 90.48% of power in all the SSTL based logic families. Where as in case of IO and total power maximum power reduction occurs in the case of SSTL2_II_DCI which is 26.59% and 56.67% with the help of clock gating.

6. Future Scope

We have implemented Gurmukhi Unicoder on 40nm technology based Virtex-6 FPGA. There is a scope to implement this Gurmukhi Unicoder on 28nm Artix-7, 28nm Kintex-7 FPGA to make the most energy efficient Gurmukhi Unicoder. We have worked up only on the SSTL based Logic Families in this paper. We can further enhance it by working on other Logic Families such as HSTL, LVDCI, LVCMOS and many more to make our circuit more energy and power efficient.

References

[1]. J. Shinde, S. Salankar, "Clock gating-A power optimizing technique for VLSI circuits", Annual IEEE India Conference (INDICON), pp: 1-4, 2011
[2]. B. Pandey, and M. Pattanaik. "Clock Gating Aware Low Power ALU Design and Implementation on FPGA." 2nd International Conference on Network and Computer Science (ICNCS), Singapore. 2013.
[3]. S. Khalsa, "Introduction to Gurmukhi". About.com. Retrieved 15 March 2013.
[4]. T. Saini, G. Lehal , and V. Kalra. Shahmukhi to Gurmukhi Transliteration System. p. 177, 2008.
[5]. B. Pandey, T. Das, T. Kumar, S. M. M. Islam, M. A. Rahman and M.E. Noor, "Low Power Devnagari Unicode Checker Design Using CGVS Approach", "Advanced Materials Research- Modern Achievements and Developments in Manufacturing and Industry, Vol. 984 - 985, pp. 1282-1285, Trans Tech Publications, Switzerland (SCOPUS Indexed), http://www.scientific.net/AMR.984-985.1282
[6]. G Singh, B. Pandey, "Simulation of CMOS IO Standard Based Energy Efficient Gurmukhi Unicode Reader on FPGA", IEEE 6th International Conference on Computational Intelligence and Communication Networks (CICN), Bhopal, 14-16 November, 2013. (Accepted)
[7]. T. Kumar, B. Pandey, and T. Das, "LVCMOS I/O Standard And Drive Strength Based Green Design on Ultra Scale FPGA", IEEE International conference on Green Computing, Communication and Conservation of Energy(ICGCE), 12-14 December, 2013.
[8]. T. Kumar, M. M. Limbu, A. Kumar, B. Pandey and T. Das "Simulation of HSTL IO Standard Based Energy Efficient Frame Buffer For Digital Image Processor", IEEE International Conference on Robotics & Emerging Allied Technologies in Engineering (iCREATE), April 22 – 24, 2014.