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Analysis of Thermal Stability of Different Counter on 28nm FPGA

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Abstract

In this paper we are presenting the power analysis for thermal awareness of different counters. The technique we are using to do the analysis is based on 28 nm FPGA technique. In this work during implementation on FPGA, we are going to analyze thermal stability of different counters in temperature range of 10^{o}C, 30^{o}C, 60^{o}C, 90^{o}C, 120^{o}C. There is 90.36% reduction in leakage power of divide by 2 counter when we scale down the temperature from 120^{o}C to 10^{o}C and 49.61% reduction in leakage power of LFSR up counter when we scale down the temperature from 120^{o}C to 10^{o}C.

Keywords: Thermal Stability, Counter, 28nm, FPGA, Ambient Temperature, Junction Temperature, Leakage Power

1. Introduction

Thermal aware design is currently gaining importance in VLSI research field. Ambient temperature plays an essential role in thermal analysis. Ambient temperature is the temperature of surroundings. Temperature creates a significant effect on leakage power dissipation. In this work we are observing the reduction in leakage power at different ambient temperature. Leakage power is the power dissipation that increases with increase in ambient temperature. In this paper we had done analysis of 5 different counters at different ambient temperature and observed the power reduction. System is designed using FPGAs which are semiconductor devices that can be reprogrammed according to requirements of user. FPGA consists of configurable logic blocks known as CLBs which are connected via interconnects that are programmable.

A. Up Down Counter

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A synchronous counter which counts up when provided high input and counts down when provided low input. Reset pin is used for resetting the current value to initial value as shown in Figure 1. Up down modes have the same priority list and only one can be use at the same time.

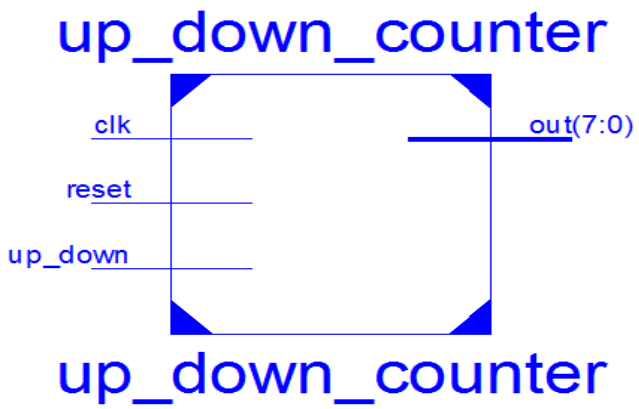

Figure 1: Up Down Counter

B. LFSR Up Down Counter

LFSR is Linear Feedback Shift Register specially used to generate random number using XOR gate and does not have all zero states for LFSR Up counter where as LFSR down counter uses XNOR gate and does not have all ones states as shown in Figure 2.

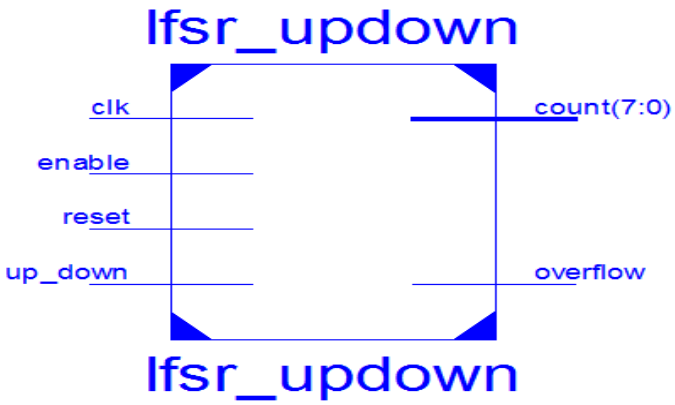

Figure 2: LFSR Up Down Counter

C. 8 bit Simple Up Counter

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8 bit Up Counters are synchronous and ideally suitable for high-speed counting applications and it is fully programmable and can be preset to any number between 0 to 255 as shown in Figure 3.

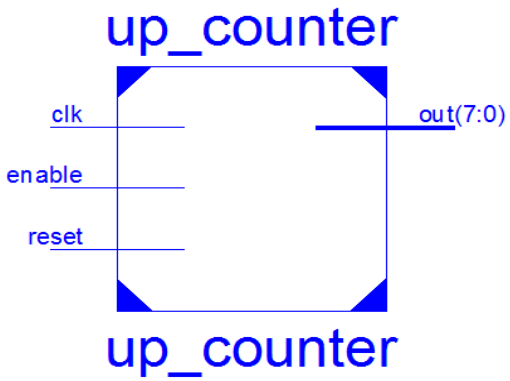

Figure 3: One Hot Counter

D. One Hot Counter

One hot counter helps the state machine to run at a faster clock rate, and also in detection of illegal states above all it is easy to design. Its nth bit is high only then the state machine is in the nth state. Schematics of one Hot counter is shown in Figure 4.

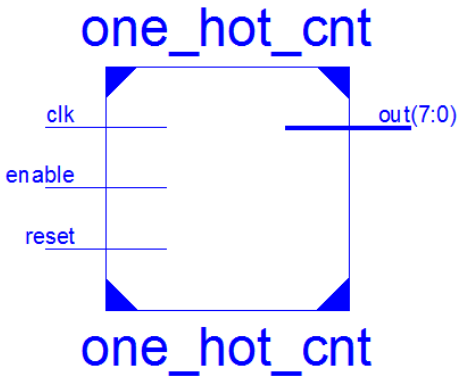

Figure 4: One Hot Counter

E. Divide by 2 Counter

This counter is basically use for division of frequency. Divide by 2 Counter is coded in Verilog, Top level schematics is generated in Xilinx ISE and shown in Figure 5.

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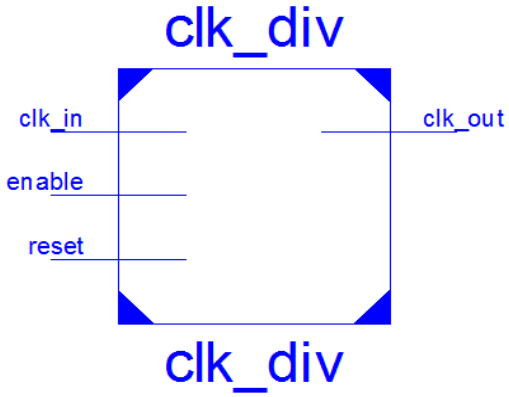

Figure 5: Divide By 2 Counter

2. Related Work

Scaling of temperature, voltage and capacitance is one of the effective energy efficient techniques on available for FPGA based design. Power optimization of Semiconductor Laser Driver is done using Voltage Scaling techniques [1]. Similar voltage scaling techniques also used in design of Mobile Battery Charge Controller Sensor on FPGA [8]. Whereas, our work is based on thermal scaling. Low Voltage Complementary Metal Oxide Semiconductor is used to make Internet of Things Enable Energy Efficient RAM Design on both 40nm and 65nm FPGA [2]. We are also using LVCMOS18 as a default IO standard on our FPGA. Other than LVCMOS, there are many other IO Standard like HSTL is used to design Energy Efficient Multiplier Design on 28nm FPGA [3]. CTHS is combination of four energy efficient technique mainly Capacitance scaling, Thermal scaling, HSTL and SSTL [4]. These combination is used design Energy Efficient Thermal Aware Image ALU on FPGA [4]. Our counter is thermal aware and energy efficient as thermal aware and energy efficient design for security on FPGA in [5]. In our work, we are also using assumption and techniques used in Energy Efficient and Thermal Aware Object Tracking on FPGA [6]. If a design use less power then it should be portable also as [7] propose a design of portable ALU Design on FPGA. Energy Efficient Design and Implementation of ALU on 40-nm FPGA is done using different techniques [9]. Clock Gating is used to reduce clock power dissipation and dynamic power dissipation too [10].

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3. Results

Table 1. Up Down Counter

Temperature(in ^{o}C)	Total power
10	0.087
30	0.099
60	0.153
90	0.320
120	0.725

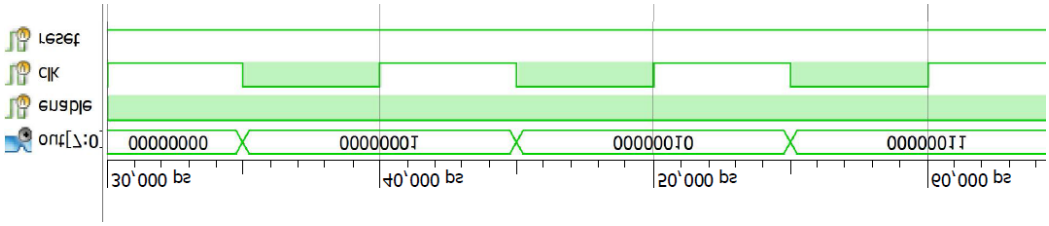

Fig. 6. Up Down Counter

When we scale down the temperature from 120 ^{o}C to 90 ^{o}C, 60 ^{o}C, 30 ^{o}C, 10 ^{o}C then there is 31.46%, 44.47%, 48.67%, 88% reduction in leakage power as shown in table 1 and figure 6.

Table 2. LFSR Up Down Counter

Temperature(in ^{o}C)	Total power
10	0.647
30	0.659
60	0.713
90	0.880
120	1.284

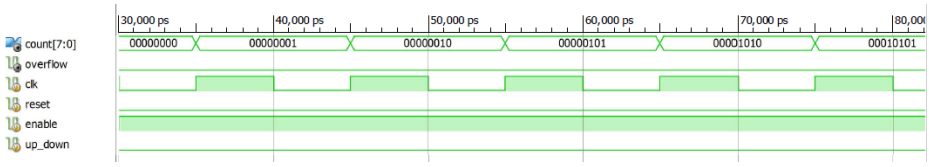

Fig. 7. LFSR Up Down Counter

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When we scale down the temperature from 120 ºC to 90 ºC, 60 ºC, 30 ºC, 10 ºC then there is 31.46%, 44.47%, 48.67%, 49.61% reduction in leakage power as shown in table 2 and figure 7.

Table 3. 8 bit Simple Up Counter

Temperature(in ºC)	Total power
10	0.096
30	0.109
60	0.163
90	0.330
120	0.734

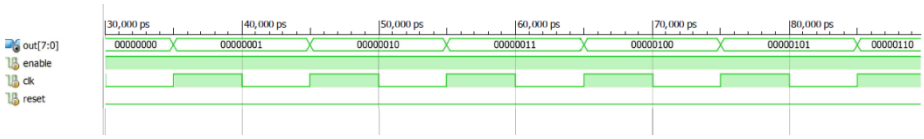

Fig. 8. 8 bit Simple Up Counter

When we scale down the temperature from 120 ºC to 90 ºC, 60 ºC, 30 ºC, 10 ºC then there is 55.04%, 77.79%, 85.14%, 86.92% reduction in leakage power as shown in table 3 and figure 8.

Table 4**.** One Hot Counter

Temperature(in ºC)	Total power
10	0.073
30	0.085
60	0.139
90	0.306
120	0.710

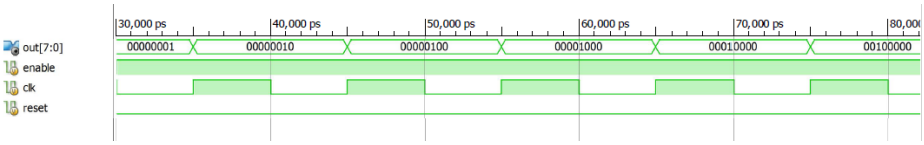

Fig. 9. One Hot Counter

When we scale down the temperature from 120 ºC to 90 ºC, 60 ºC, 30 ºC, 10 ºC then there is 56.90%, 80.42%, 88.02%, 89.71% reduction in leakage power as shown in table 4 and figure 9.

Table 5. Divide By 2 Counter

Temperature(in ºC)	Total power
10	0.068
30	0.081
60	0.135
90	0.302
120	0.706

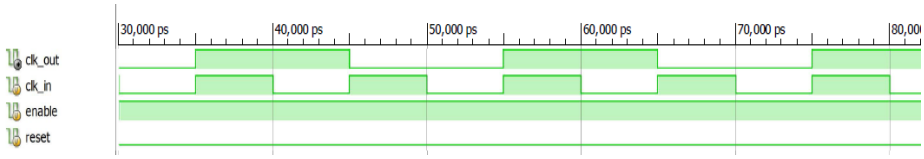

Fig. 10. Divide By 2 Counter

When we scale down the temperature from 120ºC to 90ºC, 60ºC, 30ºC, 10ºC then there is 57.22%, 80.87%, 88.52%, 90.36% reduction in leakage power as shown in table 5 and figure 10.

4. Conclusion

We can now conclude that of all the counters, Divide by 2 counter is best suited counter that is thermal aware energy efficient counter whose leakage power reduction is 90.36% when temperature falls from 120ºC to 10ºC whereas LFSR up counter is the counter whose leakage power reduction is lowest from all the counters mentioned above that is 49.61% when ambient temperature falls from 120ºC to 10ºC. Leakage power is directly proportional to temperature.

5. Future Scope

In this we are doing analysis on 28nm FPGA technique but in future we can also work on 20nm FPGA, 15nm FPGA, 7nm FPGA technique. In this work, we have taken range of ambient temperature is 10ºC to 120ºC, there is future scope to broad the range of

ambient temperature. We can also analyze the thermal stability of other counters like Gray counter, divide by 3 counter and many more.

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