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Smart Communication Network design with application of Energy Efficient Digital Clock for Monitoring of Time -To-Live

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Abstract. We are using term smart in two contexts, one context it is able to monitor Time to Live (TTL) with integration of digital clock in network and other context is energy efficiency that comes with design of energy efficient digital clock using HSTL IO standards available on Virtex-5 FPGA. Digital clock will trigger alarm when it current value reaches nearer to TTL and alarm will continue when it goes beyond TTL. This work also deals with a research gap that electronics designer never bother about selection of Input Output Standards. Current researcher focus only on efficient coding but never focus on selection of energy efficient IO standards. After testing and implementation phase of digital clock, we conclude that HSTL-II is the most efficient in term of energy efficiency and HSTL-III18 is the least efficient in term of energy efficiency.

Keywords: Energy Efficient, Digital Clock, Time-To-Live (TTL), Communication Network, HSTL IO Standards, FPGA

1 Introduction

In wireless or optical communication, one thing is common that time-to-live (TTL) is the quantitative measure of hops that limits number of packet permitted to travel before router throw away those packets [1]. A packet is the basic unit of wireless and optical communications networks [1]. The lowest time unit of this Digital clock is synchronize with time taken by packet to move from one hops to next.

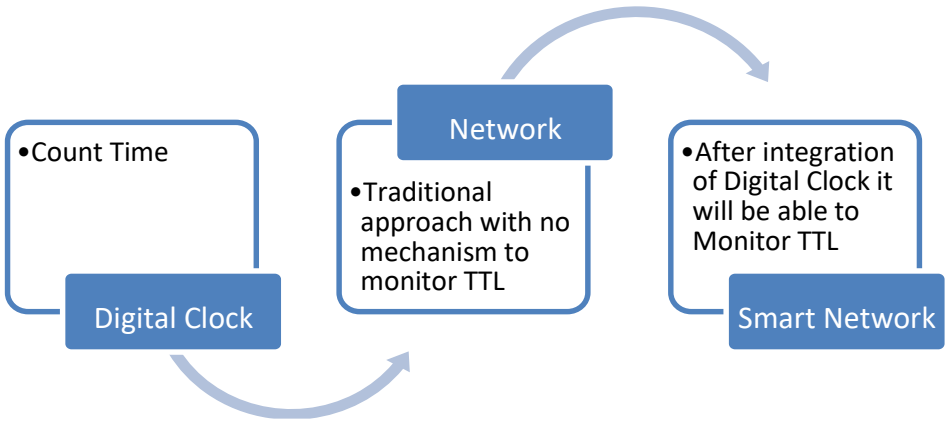

Fig. 1. Digital clock play a crucial role in Transformation of Common Network into Smart Network

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In order to display the time-to-Live, our digital clocks use display system available in Virtex-5 FPGA. Digital clock is integrated into network to count time and it will alarm when it current value reaches nearer to time to live and alarm will continue when it goes beyond TTL as shown in Figure 1. Digital clocks are very small and inexpensive devices [2]. Therefore this integration enhance economic feasibility and operational feasibility of our novel proposed design. Since digital clock is integral part of this green network design. That's why if digital clock will be energy efficient then overall network system will energy efficient network or become greener than existing system.

Table 1. Variation in Power Dissipation with Variation in IO Standards

IO Standard	IO Power
HSTL-I	15.629
HSTL_II	8.137
HSTL_III	25.076
HSTL-III18	30.353

We also found a research gap that electronics designer never bother about selection of Input Output Standards. They focus only on efficient coding but never focus on selection of energy efficient IO standards. In this work, we are using the 4 available option of HSTL IO standards and study power dissipation of all these IO standard when it integrate inside digital clock as shown in Table 1. We find that HSTL-II is the most efficient in term of energy efficiency and HSTL-III18 is the least efficient in term of energy efficiency.

2 Related Work

In [3], digital clock is used in real time delay application for digital circuit. Time to live is also delay, we are extending this FPGA based approach discussed in [3] for achieving our design goal. HSTL play an important role in simulation of energy efficient frame buffer for digital image processor [4]. HSTL IO standard has already used in energy efficient Punjabi Unicode reader design and its implementation on FPGA [5]. In CTHS Based Energy Efficient Thermal Aware Image ALU Design on FPGA [6], H stands for HSTL IO standards. HSTL play main role in design of energy efficient design Image ALU [6]. That's why we are using HSTL IO standard to achieve energy efficiency in our digital clock design. There are other application scope ofdigital clock too. These are Object Tracking [7], portable design [8] and digital signal processing [9]. Gaurav et al. focuses on different low power techniques related to SSTL IO standards and various others [10, 11, 12]. Sakshi et al. designed the green ECG machine using various logic families and compares them at different frequencies [13].

3 Data Analysis and Interpretation

3.1 Clock, Logic and Signal Power Dissipation of Digital Clock

Table 2. Values of Clock, Logic and Signal at different Frequencies

Frequency in GHz	0.01	0.1	1	10	100
Clocks	0.003	0.006	0.031	4.693	5833.156
Logic	0.000	0.001	0.008	0.053	0.300
Signals	0.000	0.001	0.015	0.138	1.335

There is 99.91%, 99.99%, 99.99% and 99.99% diminution in the clock when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 82.33%, 97.33%, 99.66% and 100% diminution in Logic when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 89.66%, 98.87%, 99.92% and 100% diminution in Signals when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Table 2 and Figure 2.

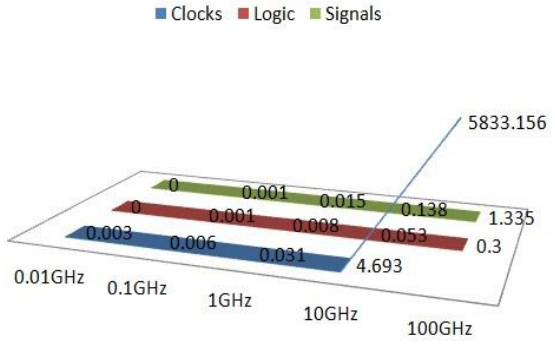

Fig. 2. Chart of Clock, Logic and Signals Power at different frequencies

3.2 IO, Leakage and Total Power Dissipation of Digital Clock for HSTL-I

Table 3. Values of I/Os, Leakage and Power at different Frequencies for HSTL-I

Frequency In GHz	0.01	0.1	1	10	100
I/Os	0.175	0.189	0.326	1.717	15.629
Leakage	0.380	0.380	0.383	0.480	0.578
Total Power	0.558	0.577	0.762	7.080	5850.998

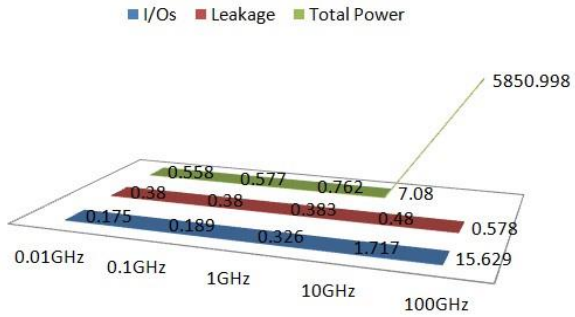

Fig. 3. Chart of I/Os, Leakage and Power at different frequencies for HSTL-I

There is 89.04%, 97.91%, 98.79% and 98.88% diminution in IOs when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 34.25%, 34.25%, 33.7% and 16.95% diminution in Leakage when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 99.87%, 99.98%, 99.9% and 99.9% diminution in Total Power when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Table 3 and Fig. 3.

3.3 IO, Leakage and Total Power Dissipation of Digital Clock for HSTL-II

Table 4. Values of I/Os, Leakage and Power at different Frequencies for HSTL-II

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Frequency in GHz	0.01	0.1	1	10	100
I/Os	0.309	0.316	0.385	1.090	8.137
Leakage	0.382	0.382	0.383	0.469	0.578
Total Power	0.694	0.705	0.822	6.442	5843.506

There is 86.60%, 95.26%, 96.11% and 96.20% diminution in IOs when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 18.85%, 33.73%, 33.91% and 33.91% diminution in Leakage when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 99.88%, 99.98%, 99.98% and 99.99% diminution in Total Power when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Table 4 and Fig. 4.

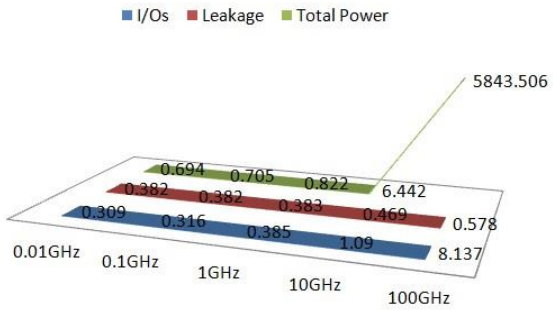

Fig. 4. Chart of I/Os, Leakage and Power at different frequencies for HSTL-II

3.4 IO, Leakage and Total Power Dissipation of Digital Clock for HSTL-III

Table 5: Values of I/Os, Leakage and Power at different Frequencies for HSTL-III

Frequency In GHz	0.01	0.1	1	10	100
I/Os	0.244	0.266	0.486	2.720	25.076
Leakage	0.381	0.381	0.385	0.498	0.578
Total Power	0.628	0.654	0.924	8.102	5860.445

There is 89.15 %, 98.06%, 98.93% and 99.02% diminution in IOs when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 13.84%, 33.39 %, 34.08 % and34.08 % diminution in Leakage when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 99.86%, 99.98%, 99.98% and99.98 % diminution in Total Power when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Table 5 and Figure 5.

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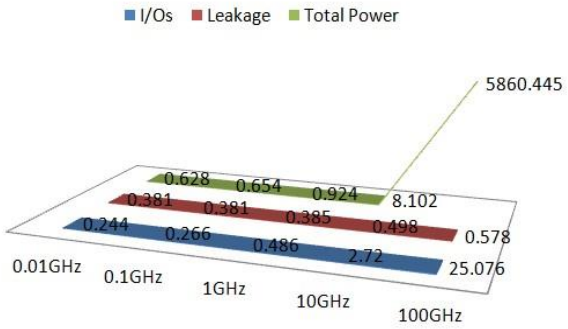

Fig. 5. Chart of I/Os, Leakage and Power at different frequencies for HSTL-III

3.5 IO, Leakage and Total Power Dissipation of Digital Clock for HSTL-III18

Table 6. Values of I/Os, Leakage and Power at different Frequencies for HSTL-III18

Frequency In GHz	0.01	0.1	1	10	100
I/Os	0.243	0.270	0.537	3.246	30.353
Leakage	0.381	0.382	0.386	0.509	0.579
Total Power	0.628	0.659	0.976	8.639	5865.722

There is 89.30%, 98.23 %, 99.11% and 99.19% diminution in IOs when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 12.08%, 33.33 %, 34.02% and 34.19 % diminution in Leakage when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 99.85%, 99.98%, 99.98% and99.98 % diminution in Total Power when we cut down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively as shown in Table 6 and Figure 6.

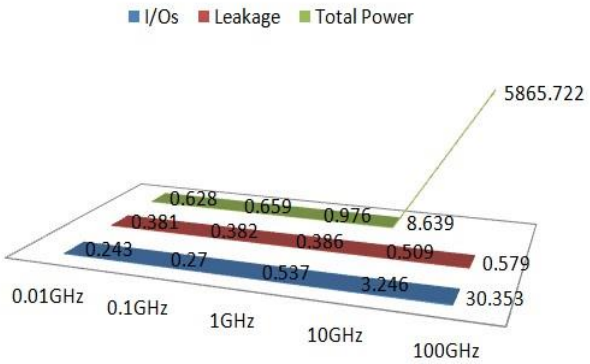

Fig. 6. Chart of I/Os, Leakage and Power at different frequencies for HSTL-III18

4 Conclusion

The power consumption of digital clock is minimum when digital clock is made using HSTL-II. Whereas, power consumption of digital clock is maximum when we use HSLT-III18 into manufacturing of digital clock. Digital clock is able to monitor time to live and it triggers alarm when it realize that TTL be already over. Our digital clock is compatible to work with frequency of 0.01GHz, 0.1GHz, 1GHz, 10GHz and 100GHz.

5 FUTURE SCOPE

This digital clocks run on mains electricity. Current design has no battery therefore it will reset every time the power is cut off. There is a future scope remains open that we can incorporate a battery backup to maintain the time during times of disconnection from the power supply. In future, we will also enhance clock range of our design below 0.01GHz and above 100 GHz.

REFERENCES

1. Time to Live definition, http://www.linfo.org/time-to-live.html
2. Digital Clock, https://en.wikipedia.org/wiki/Digital_clock
3. Krishna, B. M., Tejaswi, P., Madhumati, G. L., & Kumar, K. V. (2014). Real Time Delay Application for Digital Circuits with Peripheral Based Digital Clock Using FPGA. International Journal of Applied Engineering Research, 9(18), 5115-5123.
4. Kumar, T., Pandey, B., Limbu, M. M., Das, T., & Kumar, A. (2014, April). Simulation of HSTL I/O standard based energy efficient frame buffer for digital image processor. In Robotics and Emerging Allied Technologies in Engineering (iCREATE), 2014 International Conference on (pp. 16-20). IEEE.
5. Pandey, B., Singh, G., Parhyar, R. S., Farooq, U., & Kumar, T. (2014, December). Simulation of HSTL IO standard based energy efficient Punjabi Unicode reader on FPGA. In Open Source Systems and Technologies (ICOSST), 2014 International Conference on (pp. 62-64). IEEE.
6. Kumar, T., Pandey, B., Mussavi, S. H. A., & Zaman, N. (2015). CTHS Based Energy Efficient Thermal Aware Image ALU Design on FPGA. Wireless Personal Communications, 85(3), 671-696.
7. Musavi, S. H. A., Chowdhry, B. S., Kumar, T., Pandey, B., & Kumar, W. (2015). Iots enable active contour modeling based energy efficient and thermal aware object tracking on fpga. Wireless Personal Communications,85(2), 529-543.
8. Kumar, T., Pandey, B., Das, T., & Chowdhry, B. S. (2014). Mobile DDR IO standard based high performance energy efficient portable ALU design on FPGA. Wireless Personal Communications, 76(3), 569-578.
9. Pandey, B., Kumar, T., Das, T., & Islam, S. M. M. (2014). Thermal Mechanics Based Energy Efficient FIR Filter for Digital Signal Processing. Applied Mechanics & Materials, (612).
10. Gaurav Verma , Sushant Shekhar, Kumar Shashi Kant, Vikas Verma, Himanshu Verma and Bishwajeet Pandey, “SSTL IO Standard Based Low Power Arithmetic Design Using Calana Kalanabhyam On FPGA” International Journal of Control and Automation, vol 9, No.4, pp. 271-278, April 2016.
11. Gaurav Verma, Manish Kumar and Vijay Khare, “Low Power Techniques for Digital System Design” Indian Journal of Science and Technology”, vol 8, issue 17, IPL063, August 2015.
12. Shivani Madhok, Gaurav Verma, Ankur Bhardwaj, Himanshu Verma, Ipsita Singh, Sushant Shekhar “Capacitance Scaling With Different IO Standard Based Energy Efficient Bio-Medical Wrist Watch Design on 28nm FGPA”, International Journal of Bio-Science and Bio-Technology, Vol. 7, No. 4, pp. 145-158, August 2015.
13. S. Aggarwal, G. Verma, R. Kumar, A. Kaur, B. Pandey, S. Singh and T. Kaur, " Green ECG Machine Design Using Different Logic Families " in Proceedings of IEEE International Conference on Communication Systems and Network Technologies (CSNT-2015), pp. 830-833, April 4-6, 2015.
14. T. Gupta, G. Verma, A. Kaur, B. Pandey, A. Singh and T. Kaur," Energy Efficient Counter Design Using Voltage Scaling On FPGA" in Proceedings of IEEE International Conference on Communication Systems and Network Technologies (CSNT-2015), pp. 816-819, April 4-6, 2015.