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Designing Green ECG Machine Based on Artix-7 28nm FPGA

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Abstract

In particular this work we checked the total power consumption of ECG machine design by applying different–different techniques like frequency, voltage and ambient temperature. At first we scaled down the voltage from 2.5 volt to 1.5 volt and found that 97.46% of reduction in total power consumption. In second we scaled down our frequency form 500 MHz to 25 MHz and found 2.99 % reduction in total power consumption. In last we scaled down our ambient temperature from 60F to 20F and found 25.61% of reduction in total power of consumption. We have implemented our designed on 28nm Artix7 FPGA Family.

Keywords: Thermal Aware Design, FPGA, Energy Efficient Design.

1. Introduction

In medical field lots of researchers are working on new medical equipment which can becomes useful to check the early detection of the disease and for routine checkup of body. Here we have designed a ECG or EKG system through FPGA technology which is helpful in observing the heart diseases. For the diagnostic system ECG is very important, also known as EKG. ECG test enclose the heart's electrical activity as shown in the figure 1. In Electrocardiography we are trying to place electrodes on the skin and try to calculate the heart activity over the period of time. So it is basically use for cardiology test. Now in this era power consumption is main concern of any electrical equipment. So we are trying to make medical equipment which will consume less power. If we design the less power consumption equipment for the medical industry then it will good for the society. In figure: 2, figure: 3 we have shown the Top Level of Schematic and RTL Schematic of ECG Machine.

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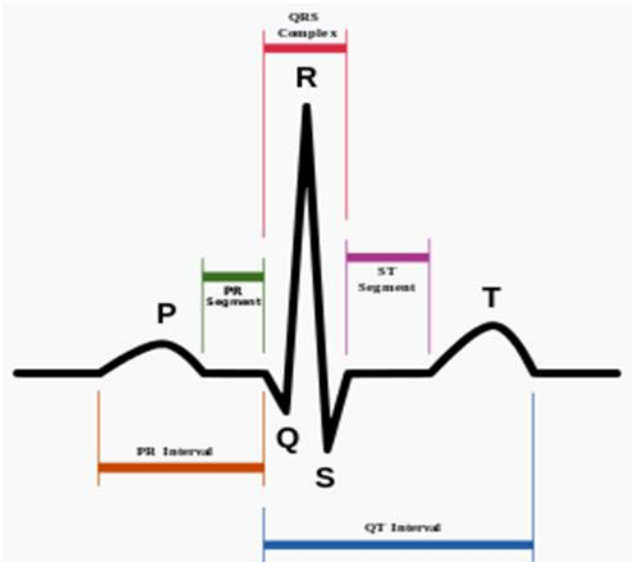

Fig. 1. ECG of a heart in normal sinus rhythm

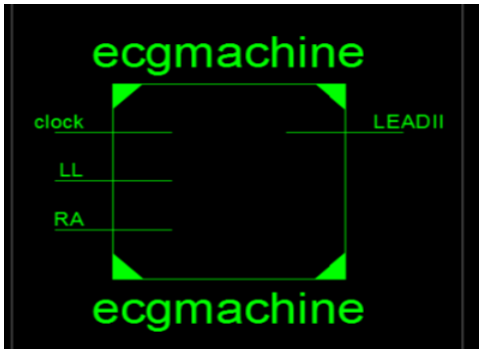

Fig. 2. Top Level of Schematic of ECG Machine

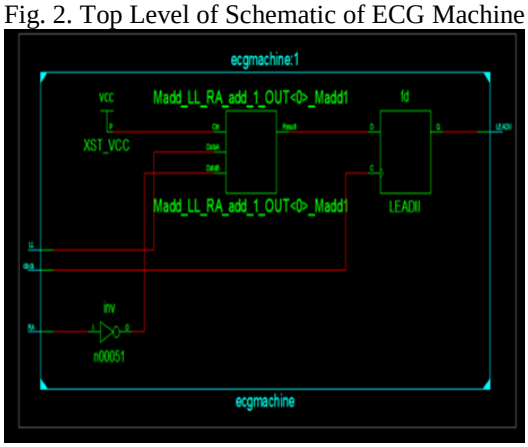

Fig. 3. RTL Schematic of ECG Machine

2. Related Survey

Energy Efficient Counter Design using Voltage Scaling On FPGA [1]. Green ECG Machine Design Using Different Logic Families [2]. A Biometric ECG Identification

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using LNF in Wireless Body Area Sensor Network [3]. Development of an embedded system and matlab based GUI for online acquisition and analysis of ECG signal [4]. Design of a Low Cost ECG system: Review [5]. Thermal Aware Low Power Universal Asynchronous Receiver Transmitter Design on FPGA [6]. Leakage Power Reduction with Various IO Standards and Dynamic Voltage Scaling in Vedic Multiplier on Virtex-6 FPGA [7]. HSTL IO Standards Based Processor Specific Green Counter [8].

3. Power Analysis

Table 1: Power Dissipation with variation in Voltage

	Clock	Logic	Signals	IOs	Leakage	Total
1.5 Volt	0.001	0.00	0.00	0.051	5.634	5.687
1.8 Volt	0.001	0.00	0.00	0.053	19.744	19.798
2.0 Volt	0.002	0.00	0.00	0.054	39.640	39.696
2.2 Volt	0.002	0.00	0.00	0.055	79.498	79.555
2.5 Volt	0.002	0.00	0.00	0.056	224.048	224.107

In the table 1 we have calculated our total power consumption at 1.5V, 1.8V, 2.0V, 2.2V and 2.5V device operating voltage respectively and found that when we scaled down the voltage form 2.5 volt to 1.5 volt then we got 97.46 % of reduction in total power. We found that there is very tiny change in the clock power. There is no change value for the Logic and Signals. We have also shown our analysis work through the bar graph as shown in the figure 4.

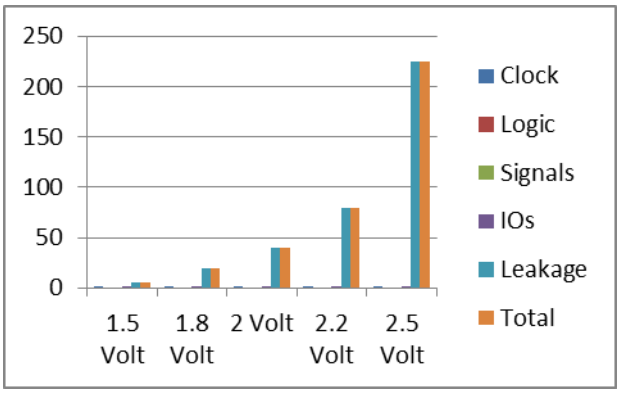

Fig. 4. Power consumption with variation in Voltage

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Table 2: Power Dissipation with variation in Frequency

	Clock	Logic	Signal	IOs	Leakage	Total
25 MHZ	0.001	0.00	0.00	0.000	1.293	1.294
200 MHZ	0.002	0.00	0.00	0.000	1.293	1.295
300 MHZ	0.009	0.00	0.00	0.009	1.293	1.312
400 MHZ	0.012	0.00	0.00	0.016	1.293	1.322
500 MHZ	0.015	0.00	0.00	0.025	1.294	1.334

In the table 2 we have applied frequency scaling technique where we use (25MHz, 200MHz, 300MHz, 400MHz, and 500MHz) following frequency rages and found when we scaled down the frequency from 500 MHz to 25 MHz then we got 2.99 % of reduction in total power consumption. We also found there is no change in logic and signal power and small changes in clock power. We have also done this analysis by the bar graph as shown in the figure 5.

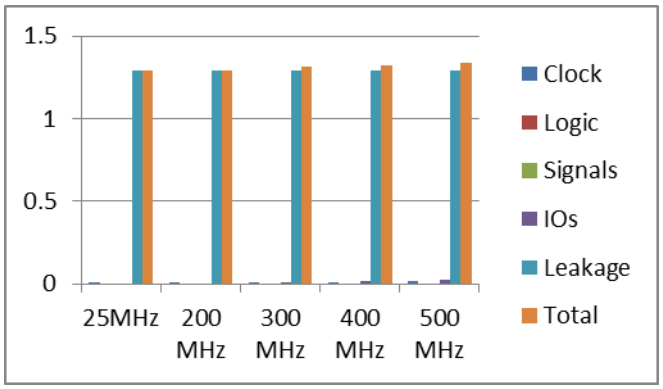

Fig. 5 Power Consumption with variation in Frequency

Table 3: Power Dissipation with variation in Ambient Temperature

	Clock	Logic	Signal	IOs	Leakage	Total
20 F	0.015	0.00	0.00	0.025	1.092	1.132
30 F	0.015	0.00	0.00	0.025	1.150	1.191
40 F	0.015	0.00	0.00	0.025	1.217	1.258
50 F	0.015	0.00	0.00	0.025	1.294	1.334
60 F	0.015	0.00	0.00	0.025	1.381	1.422

In Table 3 we calculated total power consumption by applying the ambient temperature techniques. We use (20 F, 30 F, 40 F. 50 F, 60 F) following temperature ranges and found when we reduced the temperature from 60 F to 20 F then we got 25.61% reduction in total power consumption. We also converted this same analysis through bar graph for better understanding as shown in figure 6.

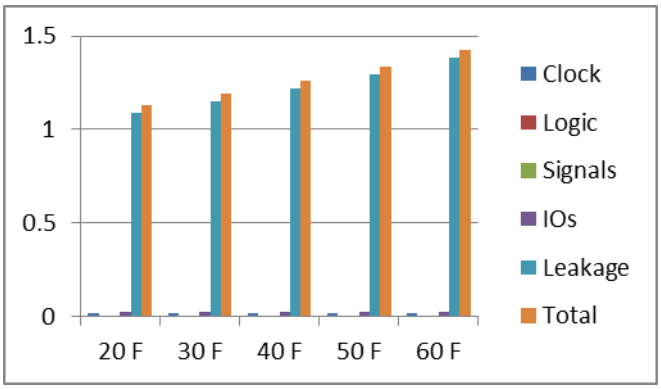

Fig. 6: Power Consumption with variation in Ambient Temperature

4. Conclusion

In this work we have implemented first voltage scaling techniques and found that when we scaled down the frequency from 2.5 volt to 1.5 volt then we reduced the power consumption by 97.46%.Secondly we implemented frequency scaling techniques and found that when we scaled down the frequency from 500 MHz to 25 MHz then we reduced the power consumption by the 2.99%.In last we applied ambient temperature techniques and found that when we scaled down the temperature from 60F to 20F then we got 25.61 % of reduction in power consumption.

5. Future Scope

In this work, ECG Design is implemented on 28nm on Airtex-7, but we have a scope to redesign this ECG machine on latest 65nm Virtex-5 and 40nm Virtex-6, 90nm Virtex-4 FPGA to make the most energy efficient ECG design. We can also take more frequency range to redesign energy efficient ECG design

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