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High Performance and Energy Efficient Traffic Light Controller Design Using FPGA

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Abstract

In this work, Verilog is used as hardware description language for implementation of traffic light controller. It shows Red, Green and Yellow color at a predefined interval. Technology scaling is used as energy efficient technique. We have used 90nm, 65nm, 40nm and 28nm technology based FPGA and then we have analyzed power consumption for traffic light controller on different FPGA. Leakage power is in range of 97.5-99% of total power consumption by traffic light controller on Virtex-7 FPGA. Signal power, clock power and IOs power are almost negligible. Power dissipation is measured on XPOWER simulator.

Keywords: Traffic Light Controller, FPGA, Verilog, Energy Efficient Design

1. Introduction

Traffic light controllers are used to control the movement of the vehicles. In the FPGA implementation of Traffic Light Controller (as shown in Fig.1-3), we are using Virtex-4, Virtex-5, Virtex-6 and Virtex-7 FPGA. Virtex-4 is 90nm technology based FPGA. Virtex-5 is 65nm technology based FPGA. Virtex-6 is 40nm technology based FPGA. Virtex-7 is 28nm technology based FPGA. LVCMOS18 is the default IO standards. 12 is drive strength as shown in Table 1. There are two inputs and 12 outputs in design under consideration. We have generated RTL schematic, technology schematic. Section 1 is introduction. Section 2 is related works on FPGA. Section 3 is results of Xpower simulator that measure power in terms of signal power, clock power, logic power, IO power and leakage power. Total power is sum of signal power, clock power, logic power, IO power and leakage power. Y denotes Yellow, R denotes Red and G denotes Green color of traffic light controller.

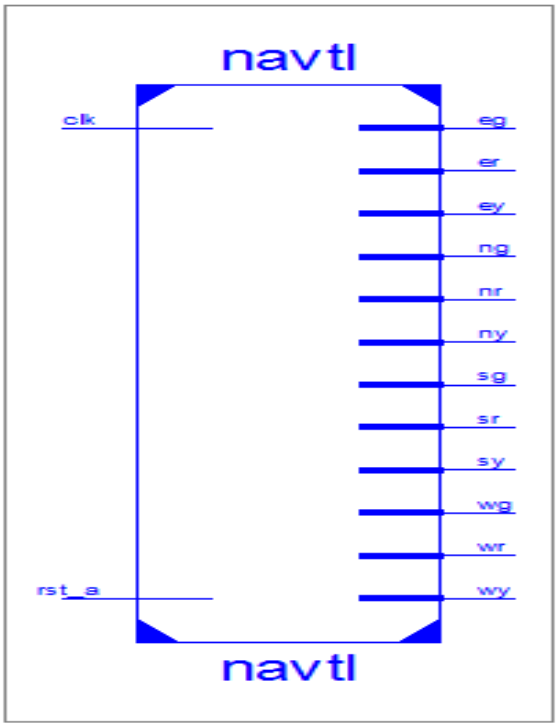

Figure 1: RTL Schematics of Traffic Light Controller

Top Level of RTL schematic is shown in Fig.1. It shows basic input required for traffic light controller and basic output required for our design under test. Clock and reset are two inputs. Whereas, there are twelve output as shown in Fig.1 and Table 1.

Table 1: IOB properties of Traffic Light Controller

IOB Name	Type	Direction	IO Standard	Drive Strength	Slew Rate
clk	IOB	INPUT	LVCMOS18		
eg	IOB	OUTPUT	LVCMOS18	12	SLOW
er	IOB	OUTPUT	LVCMOS18	12	SLOW
ey	IOB	OUTPUT	LVCMOS18	12	SLOW
ng	IOB	OUTPUT	LVCMOS18	12	SLOW
nr	IOB	OUTPUT	LVCMOS18	12	SLOW
ny	IOB	OUTPUT	LVCMOS18	12	SLOW
rst_a	IOB	INPUT	LVCMOS18		
sg	IOB	OUTPUT	LVCMOS18	12	SLOW
sr	IOB	OUTPUT	LVCMOS18	12	SLOW
sy	IOB	OUTPUT	LVCMOS18	12	SLOW
wg	IOB	OUTPUT	LVCMOS18	12	SLOW
wr	IOB	OUTPUT	LVCMOS18	12	SLOW
wy	IOB	OUTPUT	LVCMOS18	12	SLOW

Internal Architecture of RTL Schematic of traffic light controller is shown in Fig. 2. This architecture shows different multiplexer, gates and other basic primitive circuits used in RTL schematic. Technology schematic of our design is shown in Fig. 3.

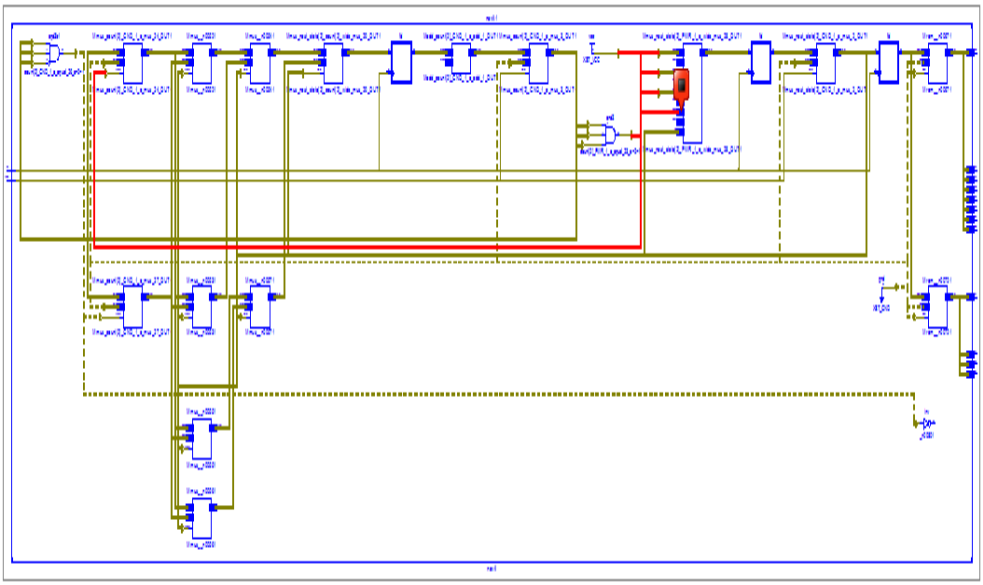

Figure 2: Internal Architecture of RTL Schematic

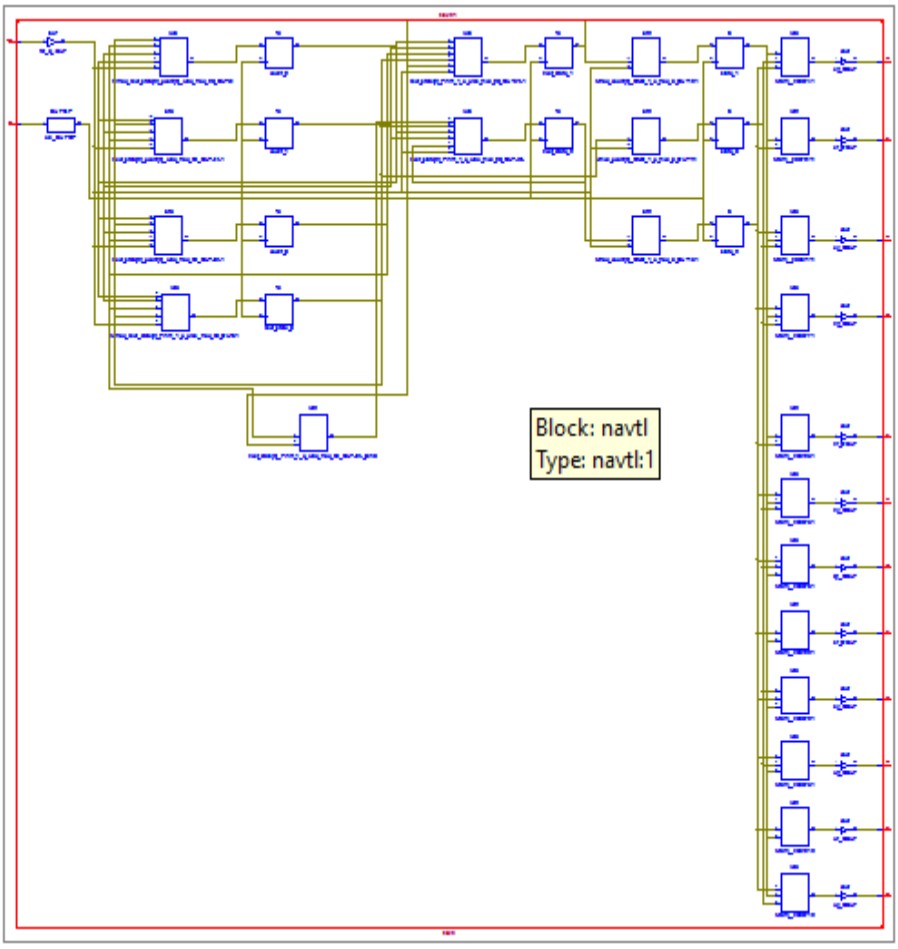

Figure 3: Technology Schematic of Traffic Light Controller

2. Related Works

A Novel Noise Free Transmission Technique is used for design of 100Gb/s Future Generation Optical Communication System on FPGA [1]. Different I/O standard and technology like thermal aware techniques and energy efficient techniques are used in Vedic multiplier design for green wireless communication on FPGA [2]. Mobile DDR IO standard is used in high performance energy efficient portable ALU design on FPGA [3]. HSTL IO Standard is used in energy efficient multiplier design on 28nm FPGA [4]. Capacitance scaling, Thermal scaling, HSTL IO standards and SSTL IO standards are used in energy efficient thermal aware image ALU design on FPGA [5]. Low power consumption techniques on FPGA is discussed for wireless devices [6]. We evaluate performance of FIR Filter and also implement on different FPGA and SOC [7]. IoTs enable Object Tracking on FPGA is discussed in [8].

3. Results

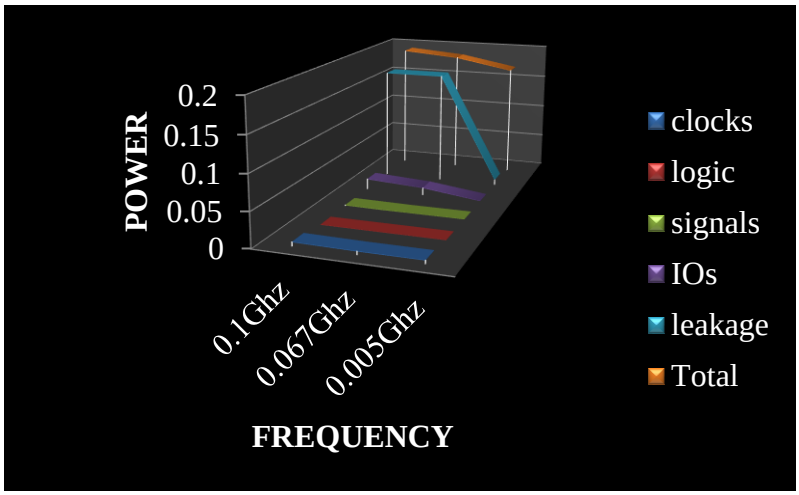

Figure 4: Power Dissipation of Traffic Light Controller with Virtex-4 FPGA

Clock power is directly proportional to frequency. Clock power increase with increase in frequency and decrease with decrease in frequency. Logic power is significant for 0.2 GHz and it becomes negligible for lower frequency as shown in Fig.4 and Table 2.

Table 2: Power Dissipation of Traffic Light Controller with Virtex-4 FPGA

Power→ Frequency↓	Clock	Logic	Signals	IOs	Leakage	Total
0.2GHz	0.007	0.001	0.001	0.032	0.167	0.208
0.1GHz	0.006	0.000	0.001	0.016	0.167	0.190
0.067GHz	0.005	0.000	0.000	0.011	0.167	0.183
0.005GHz	0.005	0.000	0.000	0.000	0.008	0.167

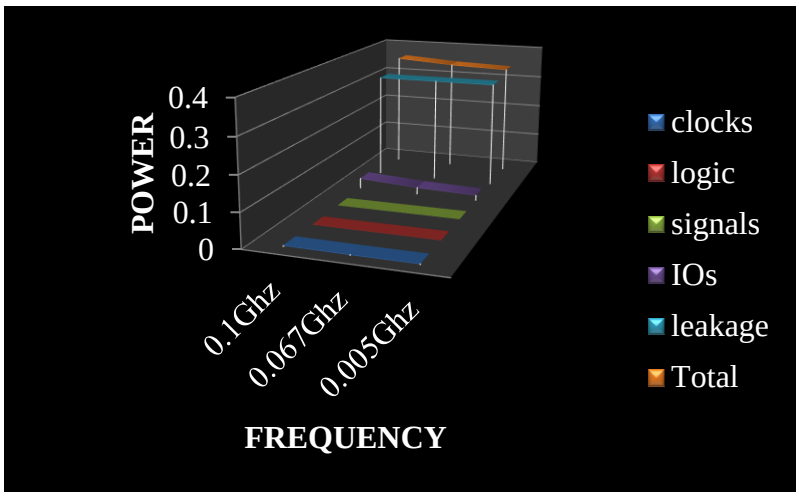

Figure 5: Power Dissipation of Traffic Light Controller with Virtex-5 FPGA

On Virtex-5, clock power is lower that clock power dissipation on Virtex-4 FPGA. Leakage power, IO Power and Total power on Virtex-5 is higher than leakage power dissipation on Virtex-4 FPGA. IOs power dissipation by traffic light controller is lower than leakage power as shown in Table 3 and Fig.5.

Table 3: Power Dissipation of Traffic Light Controller with Virtex-5 FPGA

Power→ Frequency↓	Clock	Logic	Signals	IOs	Leakage	Total
0.2Ghz	0.005	0.001	0.001	0.064	0.321	0.392
0.1Ghz	0.003	0.000	0.000	0.032	0.321	0.357
0.067Ghz	0.002	0.000	0.000	0.021	0.321	0.345
0.005Ghz	0.002	0.000	0.000	0.016	0.321	0.339

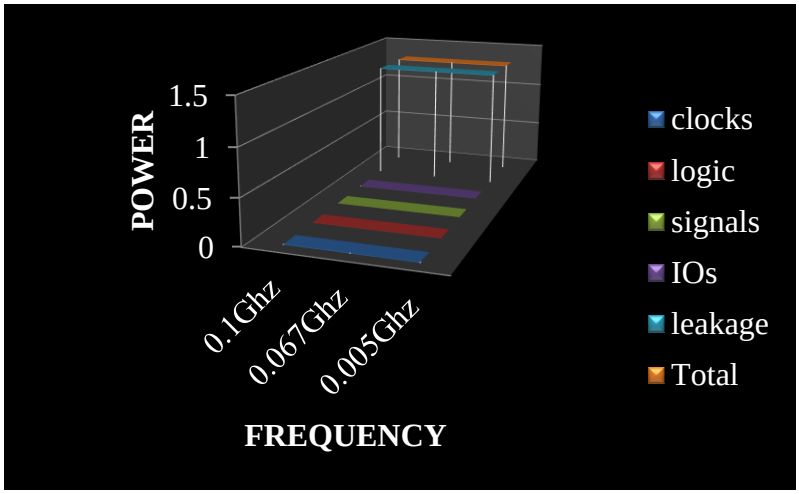

Figure 6: Power Dissipation of Traffic Light Controller with Virtex-6 FPGA

Leakage power is a maximum contributor in total power dissipation by traffic light controller on Virtex-6 FPGA. Clock power is the second most contributor in total power

dissipation. Logic, Signals and IOs power dissipation by traffic light controller is negligible as shown in Fig. 6 and Table 4.

Table 4: Power Dissipation of Traffic Light Controller with Virtex-6 FPGA

Power→ Frequency↓	Clock	Logic	Signals	IOs	Leakage	Total
0.2Ghz	0.006	0.000	0.000	0.001	1.293	1.301
0.1Ghz	0.003	0.000	0.000	0.001	1.293	1.297
0.067Ghz	0.002	0.000	0.000	0.000	1.293	1.295
0.005Ghz	0.002	0.000	0.000	0.000	1.293	1.295

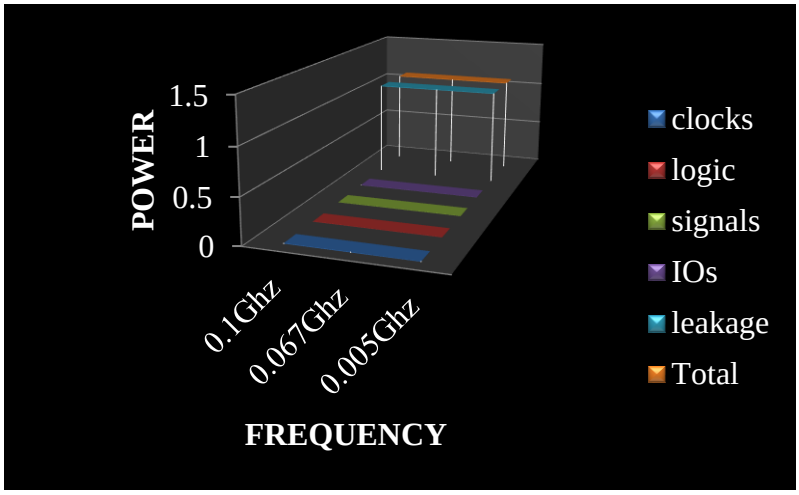

Figure 7: Power Dissipation of Traffic Light Controller with Virtex-6 Low Power FPGA

Virtex-6 Low Power FPGA has low power dissipation than the simple Virtex-6 FPGA especially in leakage power dissipation. Clock, logic, signals and IOs power dissipation are almost equal as shown in Fig.7 and Table 5.

Table 5: Power Dissipation of Traffic Light Controller with Virtex-6 Low Power FPGA

Power→ Frequency↓	Clock	Logic	Signals	IOs	Leakage	Total
0.2Ghz	0.006	0.000	0.000	0.001	1.065	1.072
0.1Ghz	0.003	0.000	0.000	0.001	1.065	1.069
0.067Ghz	0.002	0.000	0.000	0.000	1.065	1.068
0.005Ghz	0.001	0.000	0.000	0.000	1.065	1.067

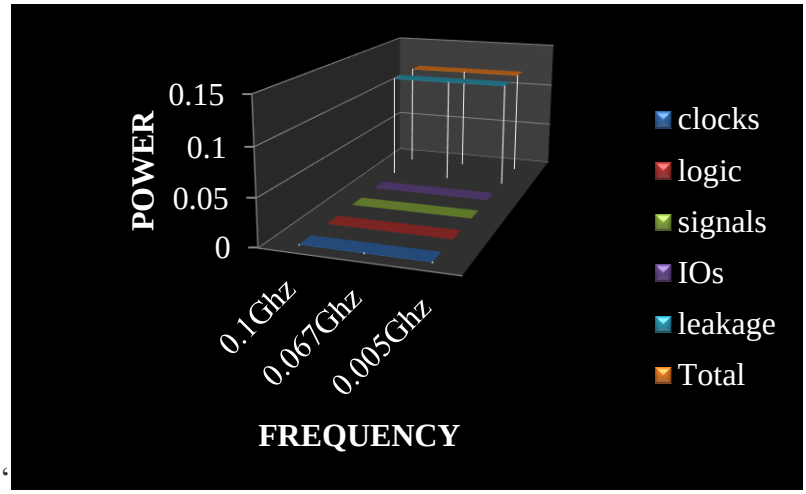

Figure 8: Power Dissipation of Traffic Light Controller with Virtex-7 Low Voltage FPGA

Leakage power is in range of 97.5-99% of total power consumption by traffic light controller on Virtex-7 FPGA as shown in Fig.8 and Table 6.

Table 6: Power Dissipation of Traffic Light Controller with Virtex-7 Low Voltage FPGA

Power→ Frequency↓	Clock	Logic	Signals	IOs	Leakage	Total
0.2Ghz	0.002	0.000	0.000	0.001	0.117	0.120
0.1Ghz	0.001	0.000	0.000	0.000	0.117	0.118
0.067Ghz	0.001	0.000	0.000	0.000	0.117	0.118
0.005Ghz	0.001	0.000	0.000	0.000	0.117	0.118

3. Conclusion and Future Scope

In this work we are using 90nm, 65nm, 40nm and 28nm technology based FPGA. In future, we shall use ultrascale FPGA for implementation of traffic light controller.

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