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Capacitance scaling based Thermal Aware Design of Waveform Generator on Virtex-6

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Abstract: This is an apporach to design of waveform generator on Virtex-6 FPGA that consume low amount of power. we have worked on different value of using capacitance scaling based thermal aware design waveform generator. There is a reduction of 69.10%, 96.77%, 99.56%, and 99.82% in IOs power as the capacitance is scale down from 50000pF to 5000pF, 500pF, 50pF and 5pF respectively.
Keywords: VHDL, FPGA, Energy Efficient,Sinusoidal Waveform Generator.

1.INTRODUCTION

we have design an electrical waveform generator for driving an electromechanical load. This approach consume low amount of power for its operation. Technique applied for doing same is capacitance scaling using Field Programmable gate Array using Xilinx software.
For the design of energy efficient we are checking the different level of ambient temperature level and capacitance scaling. We have analyzed the varying the different level of temperature to develop the energy efficient waveform generator. A waveform generator is a piece of electronic test equipment used to generate electrical waveforms. In this paper we have to use Virtex-6 FPGA family to making energy efficient waveform generator. For this model design we have coded in VHDL.

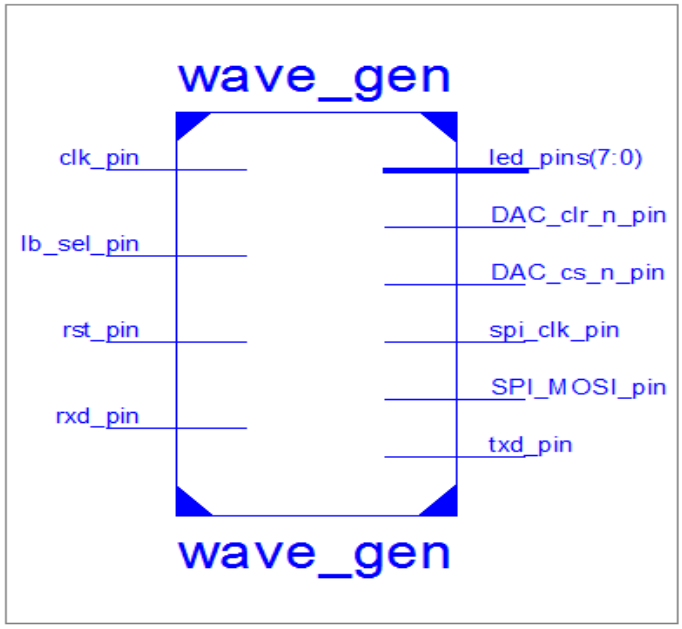

Figure 1 Top Level Schematic of Waveform Generator

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Top level Schematic of Waveform Generator is shown in Figure 1.It has four input port such as clk_pin, lb_sel_pin, rst_pin, rxd_pin and six output port such as led pins (7:0), DAC_clr_n_pin, DAC_cs_n_pin, spi_clk_pin, SPI_MOSI_pin, txd_pin.

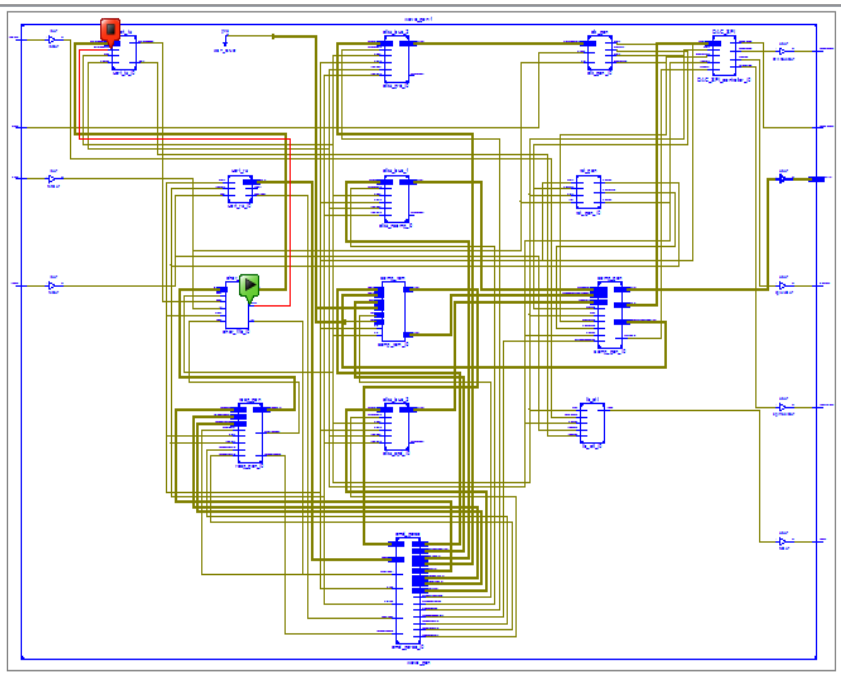

Figure 2 RTL Schematic of Waveform Generator as shown.

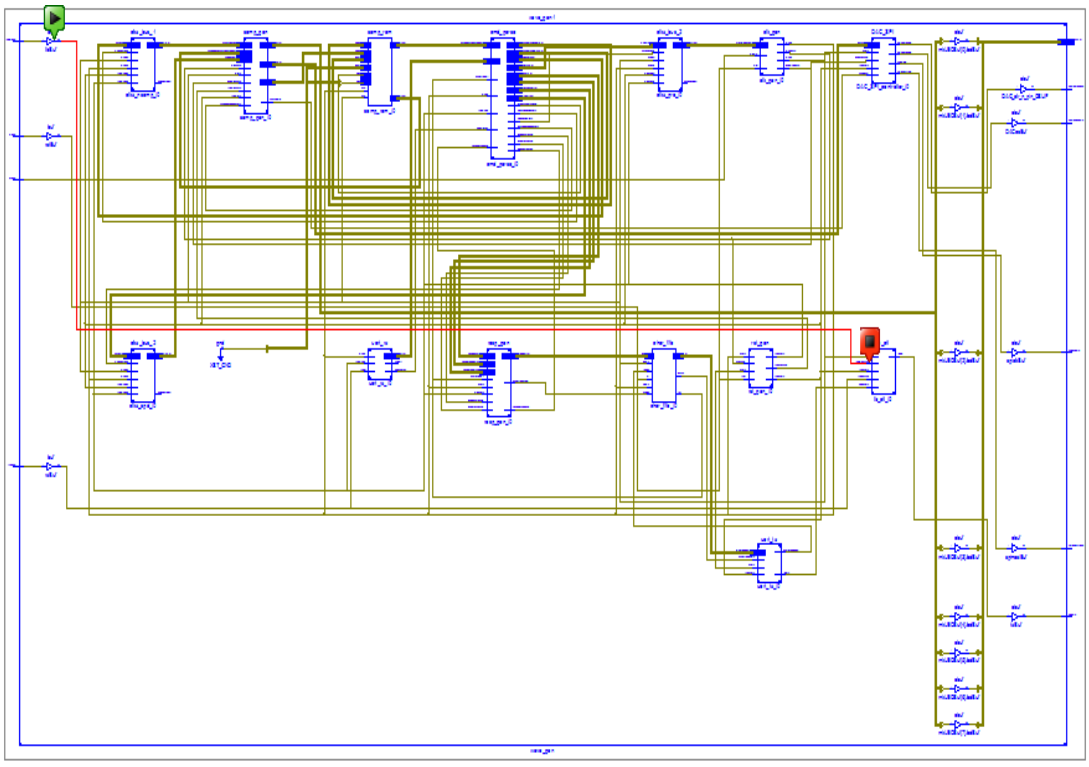

Figure 3 Internal Architecture of Technology Schematic of Waveform Generator.

2. RELATED WORK

Some researcher has designed low power clock using capacitance scaling [1]. Some of the researcher has done work on Capacitance Scaling Based Low Power Comparator Design on 28nm FPGA [2]. Some researcher has designed FPGA Based Low Power ROM Design Using Capacitance Scaling [3]. Some other researcher has work done on Capacitance scaling based energy efficient FIR filter for digital signal processing [4]. Most of the researcher has done work on the LVTTL IO standards and capacitance scaling based energy efficient ALU design on FPGA [5]. Some author has designed LOTs enable active contour modeling based energy efficient and thermal aware object tracking on FPGA [6]. Some another researcher has work done on Thermal and power aware Internet of Things enable RAM design on FPGA [7]. Some scientists has worked on LVCMOS based thermal aware energy efficient vedic multiplier design on FPGA [8]. Another researcher has done work on Thermal aware low power universal asynchronous receiver transmitter design on FPGA [9]. Some other researcher has done work on the CTHS based energy efficient thermal aware image ALU design on FPGA [10]. In our work we are using different value of capacitance to make energy efficient thermal aware design waveform generator on FPGA.

3. RESULTS AND DISCUSSION

Table 1 IOs Power Dissipation for different capacitance.

Capacitance	IOs Power
5pF	0.002
50pF	0.005
500pF	0.037
5000pF	0.355
50000pF	1.149

There is a reduction of 69.10%, 96.77%, 99.56%, and 99.82% in IOs power as the capacitance is scale down from 50000pF to 5000pF, 500pF, 50pF and 5pF respectively as shown in Table 1 and Figure 4.

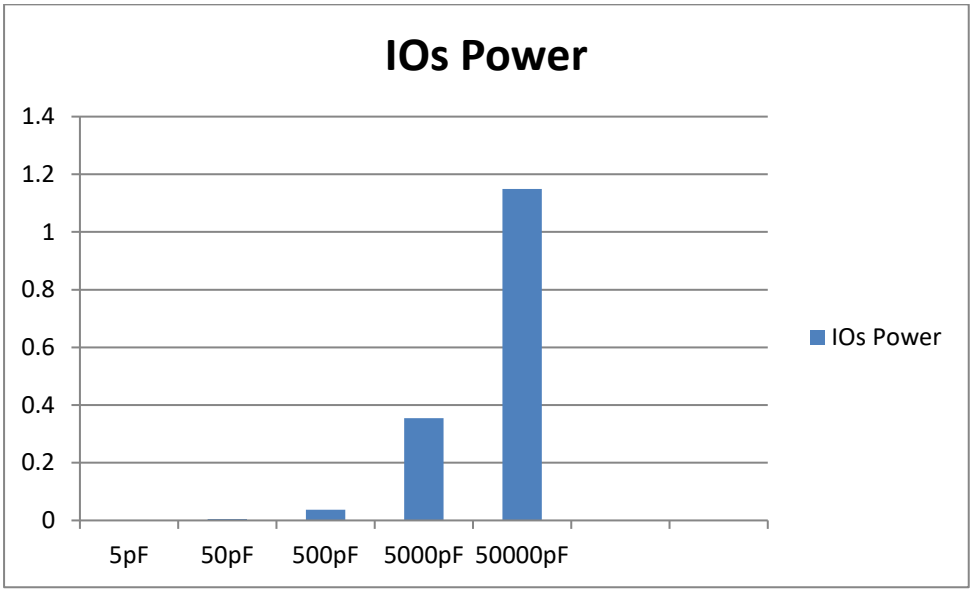

Figure 4 Graph of IOs power of different value of capacitance.

In this paper we can be used for output load capacitance value range from 0pF to 1000000pF but here we have to use up to 50000pF due to junction temperature consideration. After 50000pF junction temperature is too much high. We cannot be considering for life of waveform generator model design.

Table 2 Leakage power on different value of ambient temperature.

Ambient Temperature^{oC}	Leakage Power(w)
10^{oC}	1.042
20^{oC}	1.093
30^{oC}	1.152
40^{oC}	1.219
50^{oC}	1.295

There is a reduction of 05.86%, 11.04%, 15.59%, 19.53% in IOs power as the capacitance is scale down from 50^{oC} to 40^{oC}, 30^{oC}, 20^{oC} and 10^{oC} respectively as shown in Table 2 and Fig.5 .

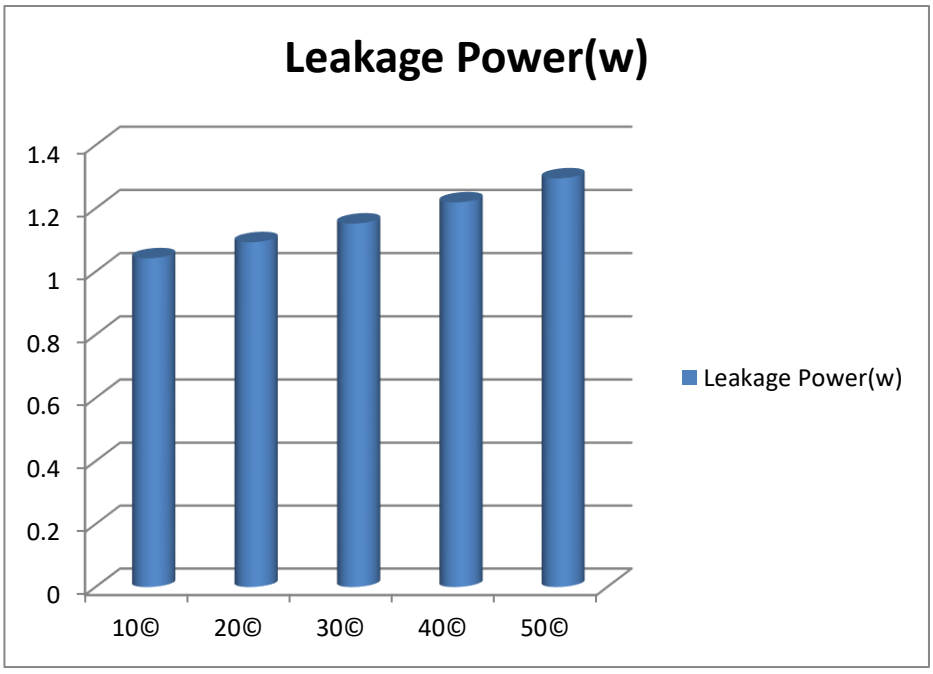

Figure 5 Graph of leakage power of different value of ambient temperature.

In this graph we have to see that slightly increase in leakage power from 1.042, 1.093, 1.152, 1.219, 1.295 with increase in ambient temperature from 10^{oC} to 50^{oC} respectively. So, ambient temperature is directly proportional to leakage power. It is nonlinear function. If temperature is increases leakage will be increase and vice-versa.

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Table 3 Different power dissipation when clock pulse period is 10 ns.

Ambient Temperature^{oC}	clocks	logic	signals	BRAMs	MMCMs
10^{oC}	0.016	0.003	0.002	0.003	0.083
20^{oC}	0.016	0.003	0.002	0.003	0.083
30^{oC}	0.016	0.003	0.002	0.003	0.083
40^{oC}	0.016	0.003	0.002	0.003	0.083
50^{oC}	0.016	0.003	0.002	0.003	0.083

There is no change in clocks, logic, signals, BRAMs, MMCMs power when ambient temperature is changes from 10^{oC} to 50^{oC} as shown in table 3 and fig.6. It is a constant value for any value of ambient temperature. So, there is no effect of temperature on clocks, logic, signals, BRAMs, MMCMs power. For any value of temperature clocks, logic, signals, BRAMs, MMCMs power is 0.016, 0.003, 0.002, 0.003, and 0.083 respectively.

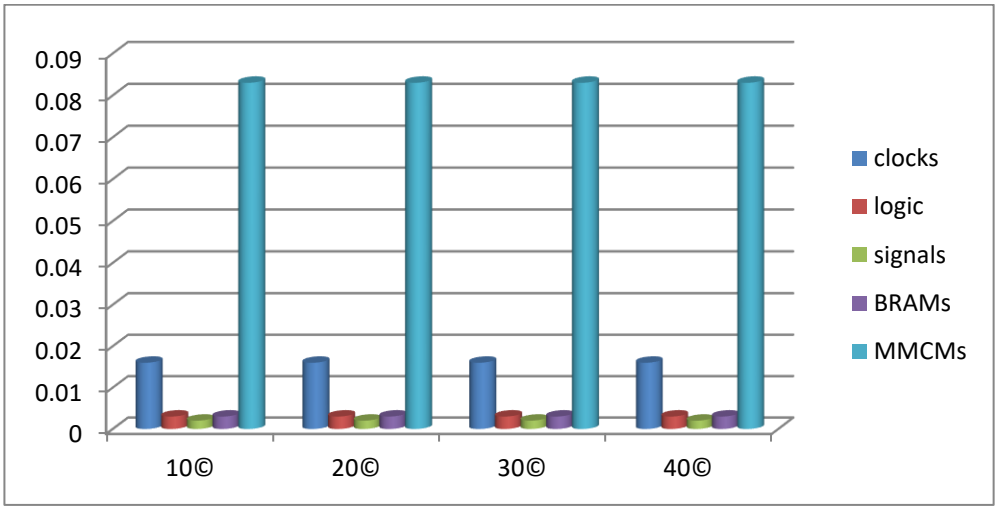

Figure 6 Graph of different power when clock pulse period is 10ns.

Here in graph we have to see that there is no change in all type of power if ambient temperature is changes from 10^{oC} to 50^{oC}.

Table 4 Estimated values of waveform generator design device utilization summary.

Device Utilization Summary (estimated values)			**[-]**
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	574	93120	0%
Number of Slice LUTs	892	46560	1%
Number of fully used LUT-FF pairs	262	1204	21%
Number of bonded IOBs	16	240	6%
Number of Block RAM/FIFO	1	156	0%
Number of BUFG/BUFGCTRLs	3	32	9%

Here we have seen that logic utilization is negligible for number of slice Registers available. It is used 574 out of 93120 Available for it. and number of slice LUTs utilization is very less value only 1%. Number of block RAM/FIFO utilization is negligible only 1 out of 156 available.

4. CONCLUSION

Here, we have concluded that there is noticeable change by varying output load at different value of capacitance and ambient temperature changes using low power Virtex-6 FPGA. Work is done in order to have an efficient design. This will help in designing low power waveform generator for efficient output.Virtex-6 gives low power readings and so is efficient for designing of not 0nly for waveform generator but various electronic designs. The capacitance scaling used from 5pF to 50000pF for clock pulse period is 10ns.

5. FUTURE SCOPE

This waveform generator model will be energy efficient and hence saves energy and power. In future we can be uses for different approaches can be made to efficient better than this. Different FPGA families like Spartan-6, Kintex-7, Airtex-7 etc. can be used for different standards like HSTL, DDR, LVCMOS, SSTL and PCI33_3 [9] etc. we have to use Frequency Scaling can also be done in future instead of varying the output load to save the energy and power.

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