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Power Efficient UART Design Using Capacitive Load on Different Nanometer Technology FPGA

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***Abstract*— In this paper, we are changing the capacitance of the UART and observing the power at different value of capacitance. As we are changing the capacitance of UART not only power but the maximum temperature and junction temperature also get affected. As the value of capacitance increases and reaches 50000 pf or above in Virtex-4, Virtex-5, Virtex-6 the capacitor of the UART burns out and for Spartan-3 and Spartan-6 when capacitance value goes to 5000 pf or above the capacitor of the UART burns out. Burning of capacitor disturbs the communication of UART over longer distance. In this paper power analysis is done on Xilinx ISE Design 14.1 and the UART code is written in Verilog Hardware Description Language. Power analysis is done by changing the capacitance of the capacitor from 5 pf to 50,000 pf at different nanometer technology based FPGA that are Virtex-4, Virtex-5, Virtex-6, Spartan-3 and Spartan-6 respectively.**

Keywords—UART, Xilinx, Capacitance, Virtex-4, Virtex-5, Virtex-6, Spartan-3, Spartan-6, Power analysis.

1. INTRODUCTION

The value of capacitance plays an important role in serial communication. Lower the value of capacitance, lesser will be drop of voltage and smoother the long distance communication. The higher value of capacitance i.e. 50000 pf or above in Virtex-4, Virtex-5, Virtex-6 , and for Spartan-3 and Spartan-6 when capacitance value goes to 5000 pf or above, UART capacitor starts burning and hence it affects the long distance communication. The change in the value of capacitance of UART is done at 1GHz frequency having a duty cycle of 50% and 1ns time period. In UART communication not only capacitance but resistance and inductance also plays a vital role. The changing value of capacitance implies mismatching of character impedance and hence causes distortion of data. The change in value of capacitance is observed on different FPGA that are Virtex-4, Virtex-5, Virtex-6, Spartan-3 and Spartan-6. The power chart of Virtex-4, Virtex-5, Virtex-6, Spartan-3 and Spartan-6 are given in Table 1, Table 2, Table 3, Table 4, Table 5, and Table 6 respectively, when the capacitance of UART is varied from 50 pf to 50,000 pf.

Table 1. Power chart of Virtex-4 when capacitance is varied from 50 (Pf) to 50,000 (Pf).

Power on chip	50 (Pf)	500 (Pf)	5,000 (Pf)	50,000 (Pf)
Clock	0.023	0.023	0.023	0.023
Logic	0.001	0.001	0.001	0.001
DCM	0.000	0.000	0.000	0.000
Signal	0.002	0.002	0.002	0.002
IOs	0.024	0.154	1.451	14.422
Leakage	0.167	0.170	0.201	0.222
Total	0.217	0.350	1.678	14.670

Table 2. Power chart of Virtex-5 when capacitance is varied from 50 (Pf) to 50,000 (Pf).

Power on chip	50 (Pf)	500 (Pf)	5,000 (Pf)	50,000 (Pf)
Clock	0.013	0.013	0.013	0.013
Logic	0.000	0.000	0.000	0.000
Signal	0.001	0.001	0.001	0.001
IOs	0.033	0.225	2.139	21.285
Leakage	0.321	0.323	0.345	0.491
Total	0.309	0.563	2.439	21.790

Table 3. Power chart of Virtex-6 when capacitance is varied from 50 (Pf) to 50,000 (Pf).

Power on chip	50 (Pf)	500 (Pf)	5,000 (Pf)	50,000 (Pf)
Clock	0.033	0.033	0.033	0.033
Logic	0.000	0.000	0.000	0.000
Signal	0.002	0.002	0.002	0.002
IOs	0.069	0.462	4.390	43.671
Leakage	1.295	1.304	1.399	1.633
Total	1.399	1.801	5.824	45.334

Table 4. Power chart of Spartan-3 when capacitance is varied from 50 (Pf) to 50,000 (Pf).

Power on chip	50 (Pf)	500 (Pf)	5,000 (Pf)	50,000 (Pf)
Clock	0.015	0.015	0.015	0.015
Logic	0.001	0.001	0.001	0.001
Signal	0.002	0.002	0.002	0.002
IOs	0.041	0.282	2.687	26.740
Leakage	0.028	0.028	0.036	0.036
Total	0.087	0.328	2.742	26.715

Table 5. Power chart of Spartan-6 when capacitance is varied from 50 (Pf) to 50,000 (Pf).

Power on chip	50 (Pf)	500 (Pf)	5,000 (Pf)	50,000 (Pf)
Clock	0.013	0.013	0.013	0.013
Logic	0.001	0.001	0.001	0.001
Signal	0.002	0.002	0.002	0.002
IOs	0.065	0.457	4.386	43.667
Leakage	0.015	0.020	0.052	0.052
Total	0.094	0.492	4.453	43.734

2. RELATED WORK

In [1] power consumption in 65nm FPGA is tested by the authors which has given a benefit in low power consumption than Virtes-4 FPGA. In [2] authors have designed CAD technique for power optimization. In this work they have tried to reduce the dynamic power dissipitation. In [3] authors using Virtex-6 FPGA have tested the capacitance of output load by implementing it on UART and they also have tested its power. In [4] authors have tried to scaled the capacitance value for energy efficient tera hertz and designed a Malayalam Unicode Reader on Virtex-6 FPGA. In [5] analysis of power consumption of BCD Adder is tested by the authors using FPGA on Xilinx ISE Design software. In[6] authors have designed a routing switch which uses low power on FPGA. In [7] authors have implemented a design using FPGA which controls phase modulation for series resonant inverters. In [8] authors have tried to low down the power with the help of 28nm FPGA on Xilinx 7 Series. In [9] authors have designed an alogorithm for online parametric identification using FPGA for resonant converters. But in our work we have tested the power of Virtex-4, Virtex-5, Virtex-6, Spartan-3, Spartan-6 FPGAs by varying the capacitance value. We also have given an impact on its change of thermal properties using Xilinx 14.1 ISE Design software.

3. POWER ANALYSIS

A. Power analysis of Virtex-4 90nm FPGA, when capacitance value changes from 50Pf to 50,000Pf.

There is no change in clock, logic, signal and dcm power in Virtex-4 when the capacitance is varied from 50Pf to 50,000Pf. The IOs power, leakage power and the total power only changes. And when the capacitance value reaches 50,000 Pf the capacitor of the UART gets burned. The change in IOs Power is shown in figure 1.

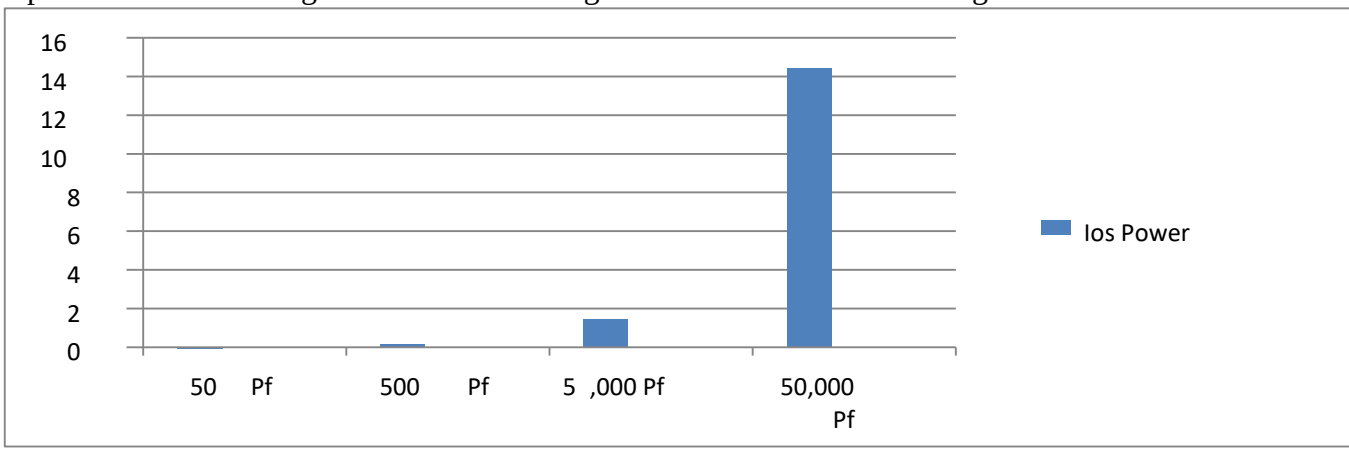

Figure 1. Change in IOs power of Virtex-4 90nm FPGA.

There is only slight change in leakage power when capacitance varies from 50Pf to 50,000Pf. The change in leakage power is shown in figure 2.

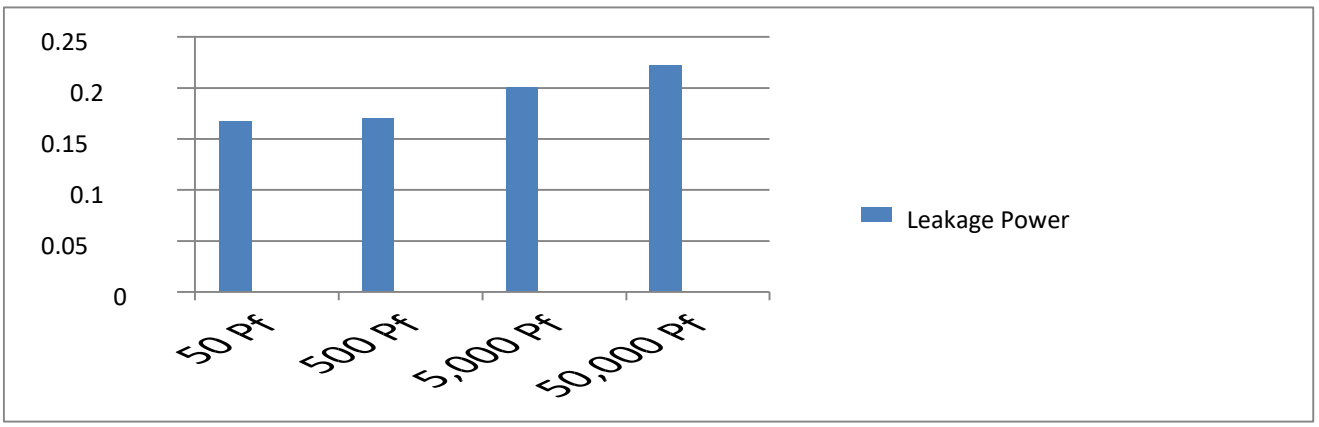

Figure 2. Change in leakage power of Virtex-4 90nm FPGA.

The total power of Virtex-4 90nm FPGA change with a very less amount on change from 50Pf to 5,000Pf, but as the capacitance changes from 5,000Pf to 50,000Pf there is a drastic increase in total power with a change of 732.538%. The total power variation of Virtex-4 is shown in figure 3.

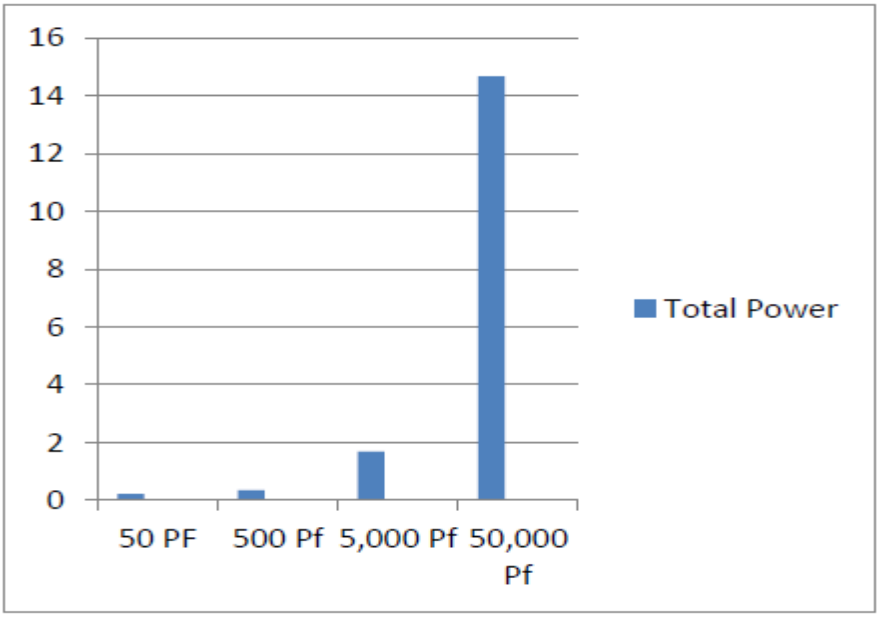

Figure 3. Change in total power of Virtex-4 90nm FPGA.

B. Power analysis of Virtex-5 65nm FPGA, when capacitance value changes from 50Pf to 50,000Pf.

In case of Virtex-5 there is also no change in clock, signal and logic power with change in capacitance value from 50Pf to 50,000Pf. But the IOs, leakage and total power changes. When the value of capacitance reaches 50,000 Pf the capacitor gets burned. The variation of IOs, Leakage and Total power is shown in figure 4, figure 5, and figure 6 respectively.

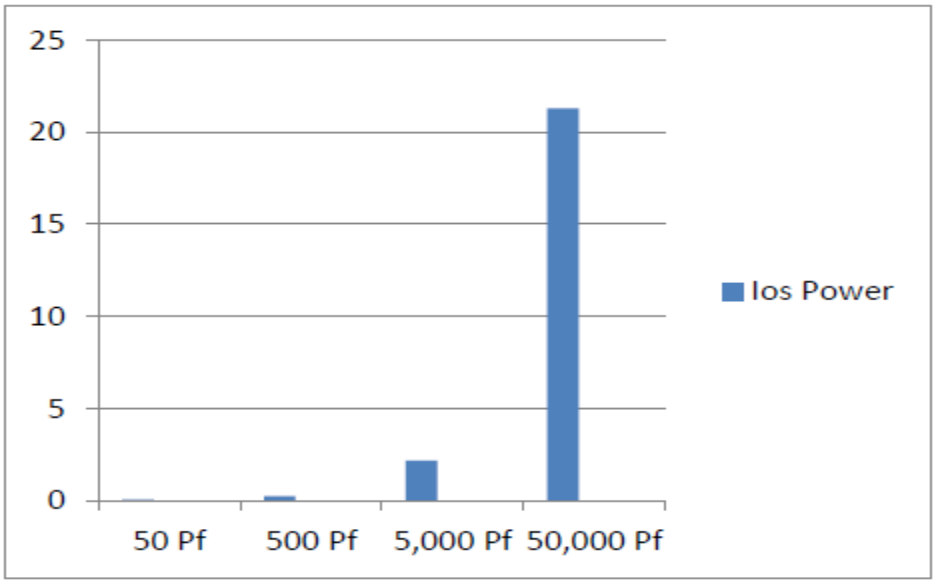

Figure 4. Change in IOs power of Virtex-5 65nm FPGA.

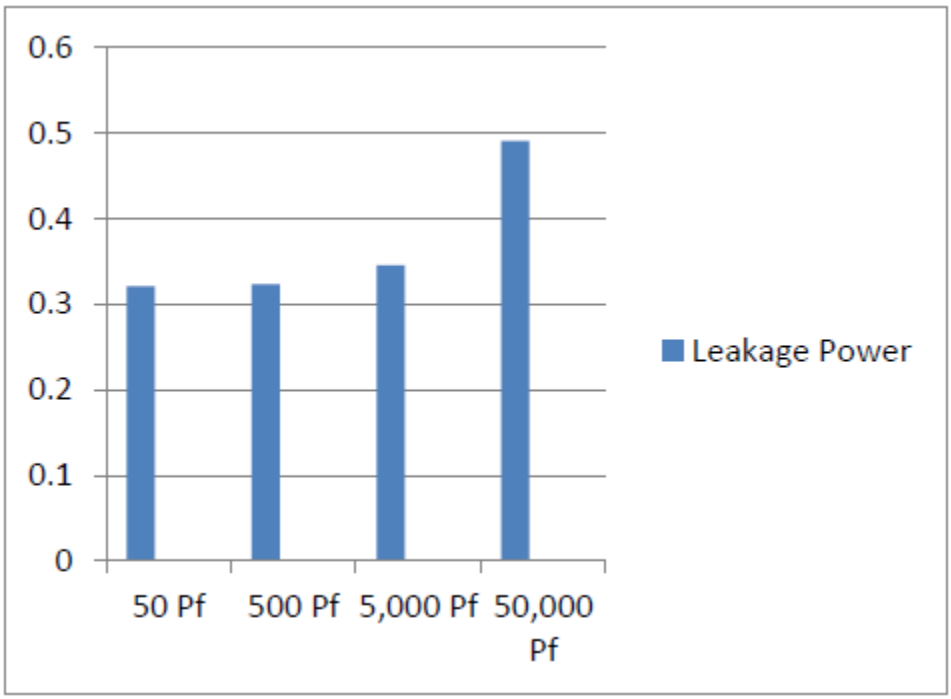

Figure 5. Change in leakage power of Virtex-5 65nm FPGA.

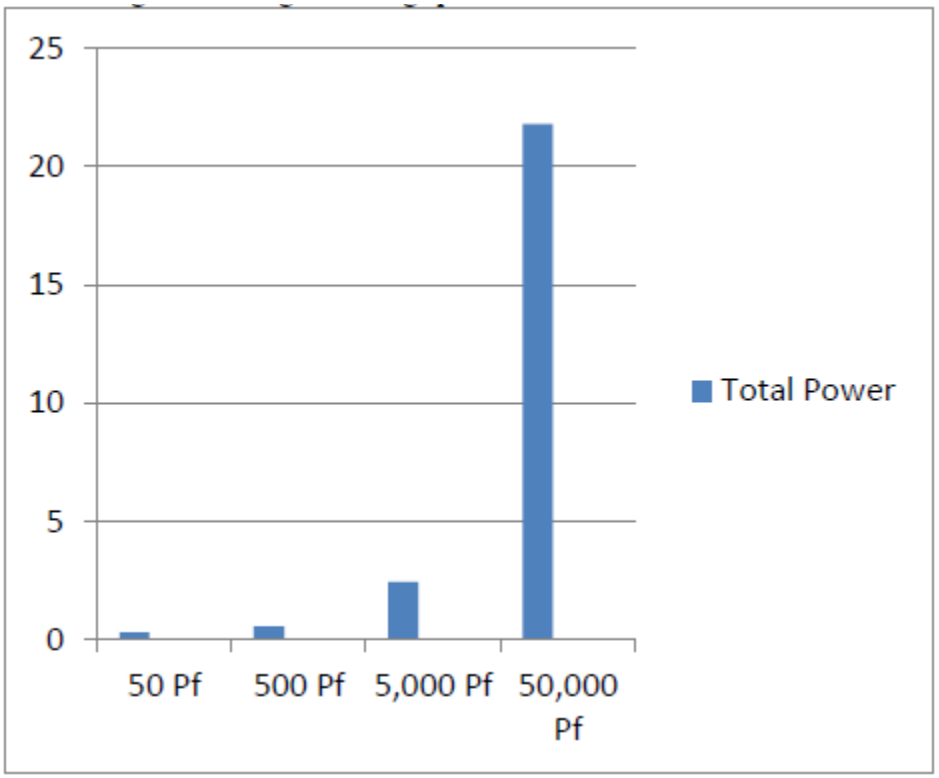

Figure 6. Change in total power of Virtex-5 65nm FPGA.

C. Power analysis of Virtex-6 40nm FPGA, when capacitance value changes from 50Pf to 50,000Pf.

In case of Virtex-6 40nm FPGA IOs, leakage and the total power is least at 50Pf and highest at 50,000 Pf. And the clock, logic and signal power not get effected with

change of capacitance value. The capacitor gets burned at 50,000 Pf. The power change in IOs is shown in figure 7.

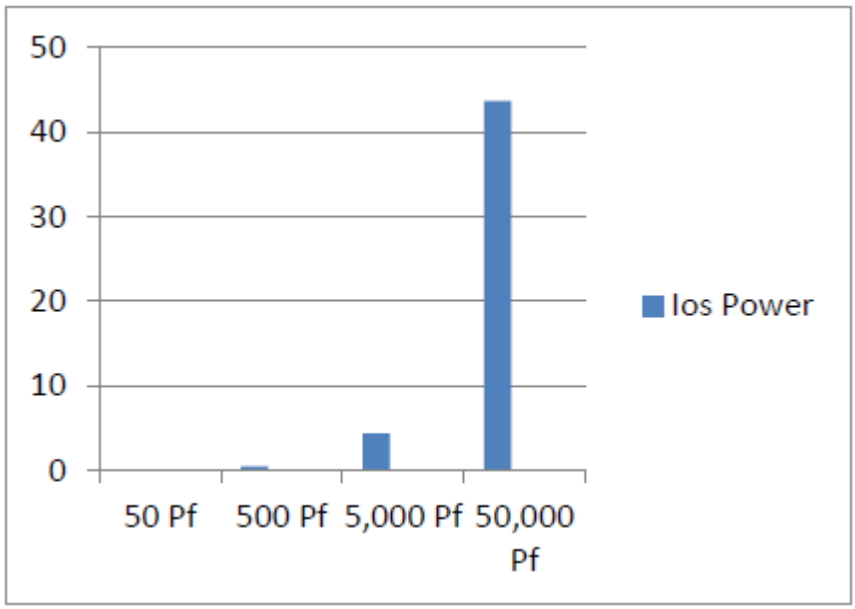

Figure 7. Change in IOs power of Virtex-6 40nm FPGA.

The change in leakage power is shown in figure 8. When capacitance is varied from 50Pf to 50,000Pf.

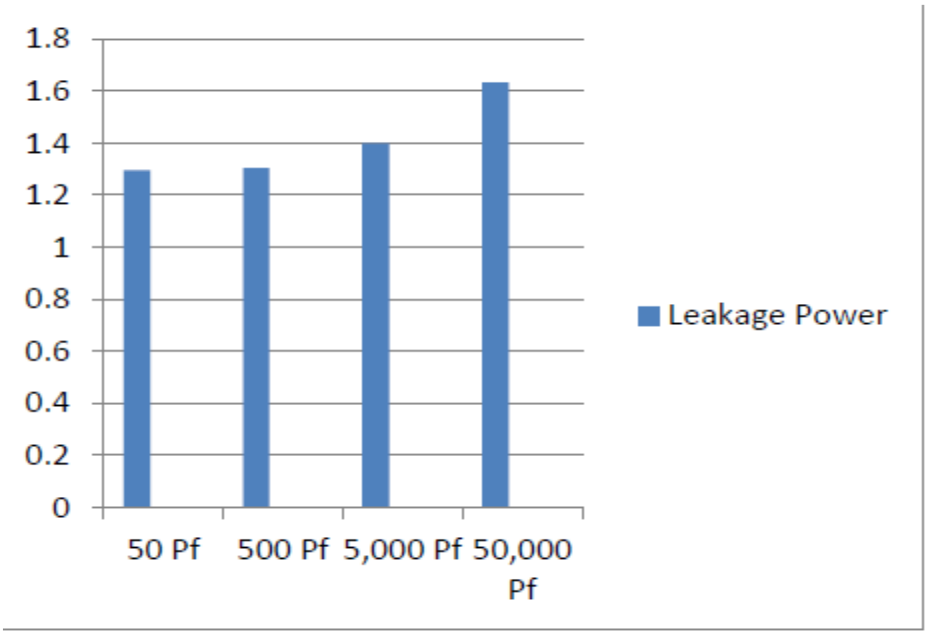

Figure 8. Change in leakage power of Virtex-6 40nm FPGA.

The power chart of total power is shown in figure 9.

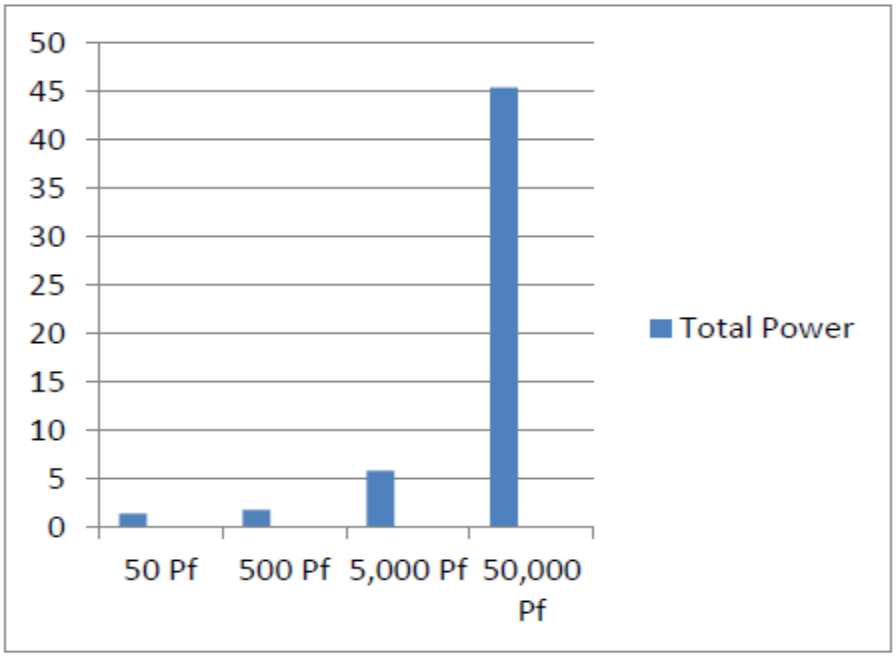

Figure 9. Change in total power of Virtex-6 40nm FPGA.

D. Power analysis of Spartan-3 90nm FPGA, when capacitance value changes from 50Pf to 50,000Pf.

There is no change in clock, logic, signal and DCM power in Spartan-3 when the capacitance is varied from 50Pf to 50,000Pf. The IOs power, leakage power and the total power only changes. And when the capacitance value reaches 5,000 Pf or above the capacitor of the UART gets burned. The change in IOs Power is shown in Fig. 10.

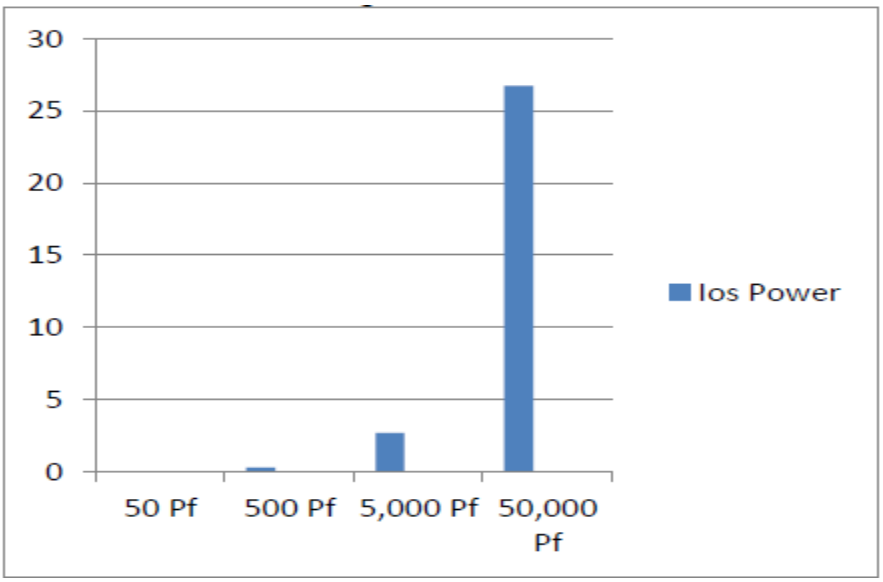

Figure 10. Change in IOs power of Spartan-3 90nm FPGA.

The leakage power of Spartan-3 is same for 50Pf and 500Pf and same for 5,000pf and 50,000Pf. The variation of leakage power is shown in Fig. 11.

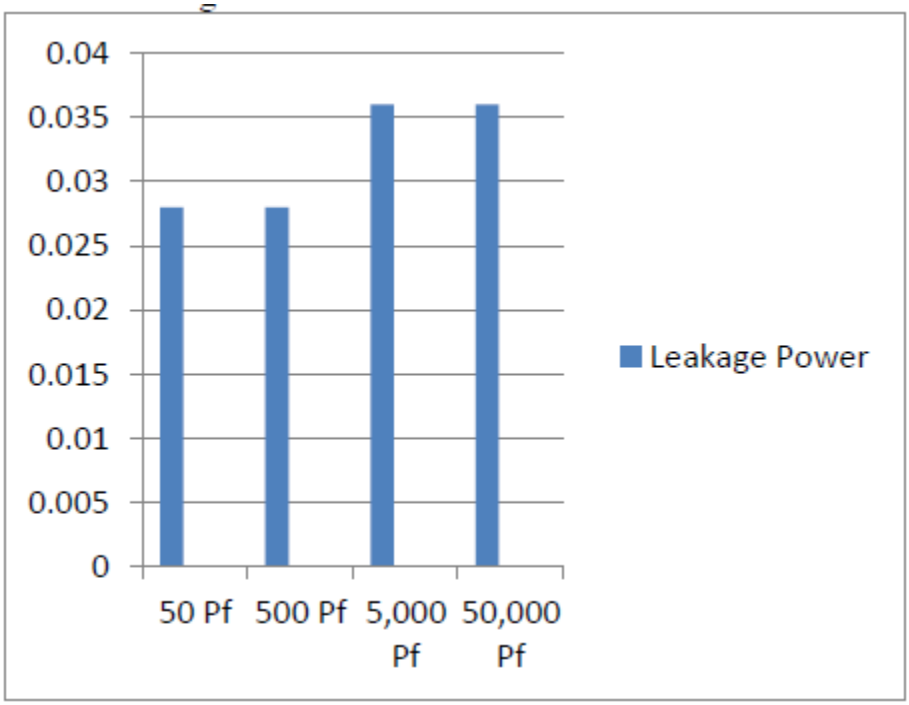

Figure 11. Change in leakage power of Spartan-3 90nm FPGA

The change in total power when capacitance changes from 50Pf to 50,000Pf is shown in figure 12.

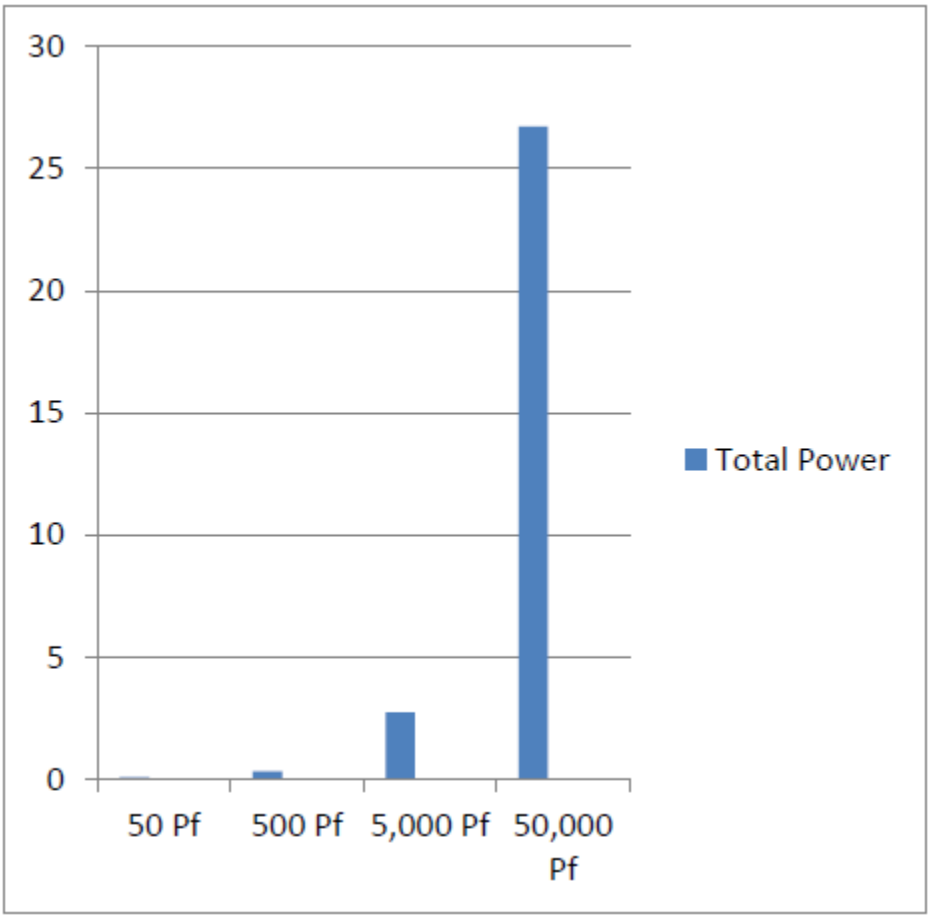

Figure 12. Change in total power of Spartan-3 90nm FPGA.

E. Power analysis of Spartan-6 45nm FPGA, when capacitance value changes from 50Pf to 50,000Pf.

In case of Spartan-6 45nm FPGA IOs, leakage and the total power is least at 50Pf and highest at 50,000 Pf. And the clock, logic and signal power not get effected with change of capacitance value. The capacitor gets burned at 5,000 Pf or above. The power change in IOs is shown in figure 13.

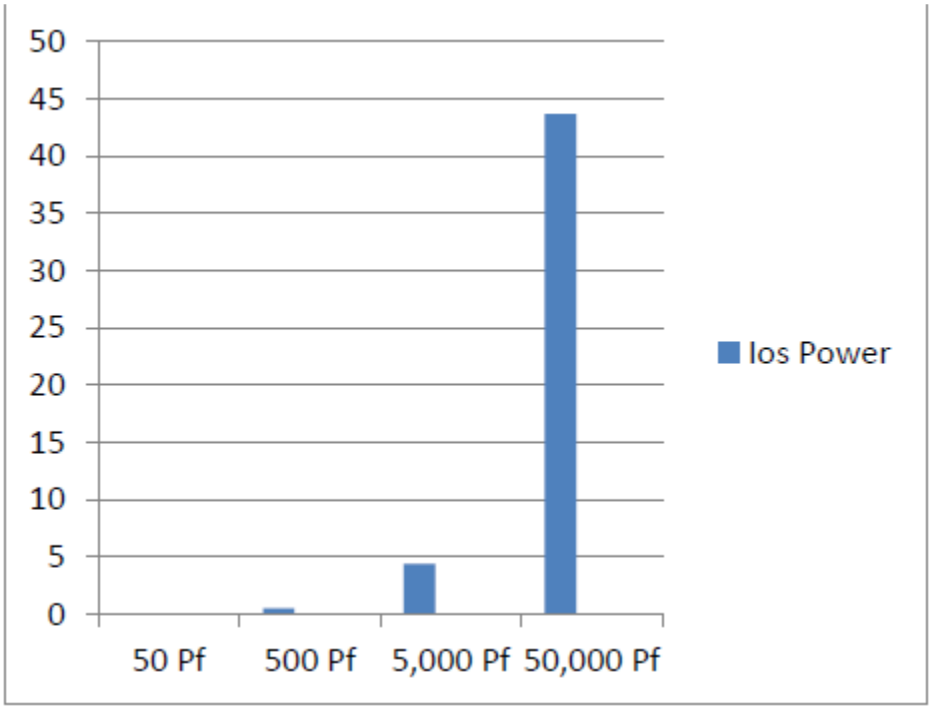

Figure 13. Change in IOs power of Spartan-6 45nm FPGA.

The change in leakage power is shown in figure 14. when capacitance is varied from 50Pf to 50,000Pf.

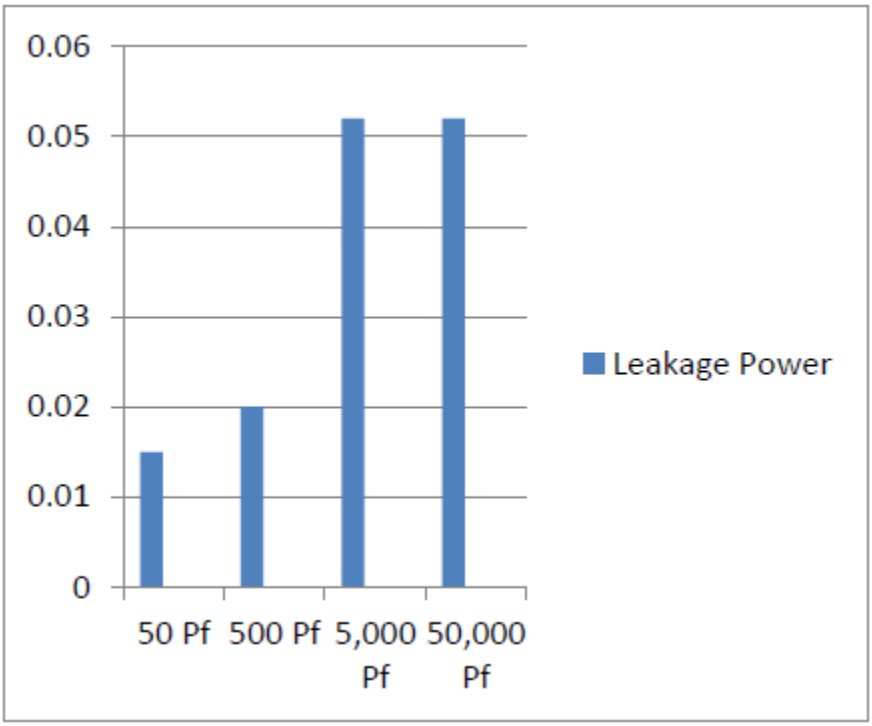

Figure 14. Change in leakage power of Spartan-6 45nm FPGA.

The power chart of total power is shown in figure 15.

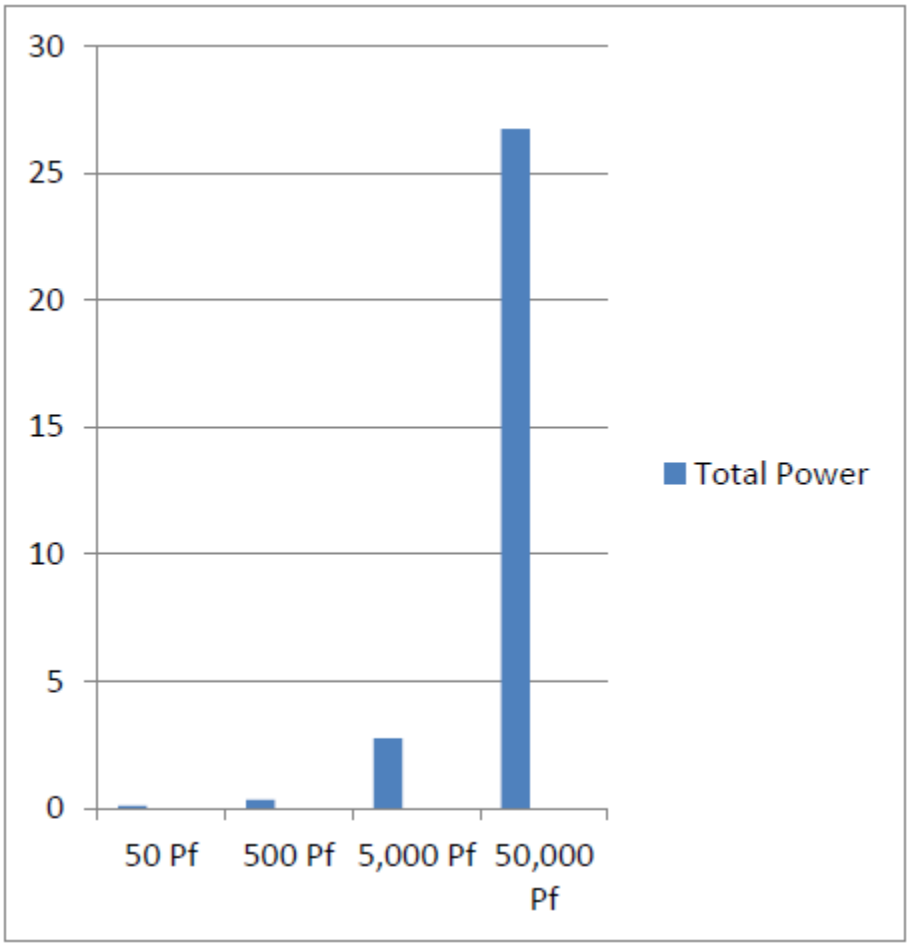

Figure 15. Change in total power of Spartan-6 45nm FPGA

4. CONCLUSION

The power efficiency of UART is analyzed on Xilinx 14.1 ISE Design in Verilog Hardware Language. The FPGAs used here are of Virtex-4, Virtex-5, Virtex-6, Spartan-3 and Spartan-6 for power comparison. The capacitance is varied from 50Pf to 50,000Pf for all FPGAs. And it is found that for all FPGAs IOs, leakage and total power is least at 50Pf and as the capacitance value reaches 50,000Pf power reaches it maximum value and also at 50,000Pf capacitance UART gets burned. Hence it is concluded as lower the capacitance value, lower the power of all FPGAs.

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