Design of Voltage Scaling Based Power-Efficient UART and its Implementation on 7-Series FPGA

[1]Keshav Kumar, [2]Bishwajeet Pandey, [3]Jason Levy, [4]Sri Chusri Haryanti, [5]D M Akbar Hussain

[1,2]*Centre of Energy Excellence, Gyancity Research Consultancy, Motihari, India*
[3]*University of Hawaii, USA*
[4]*Faculty of Information Technology, Universitas YARSI, Jakarta, Indonesia*
[5]*Aalborg University, Denmark*

thekeshavkumar1993@gmail.com, gyancity@gyancity.com, jley@hawaii.edu, chusri.haryanti@gmail.com, akh@et.aau.dk

Abstract

In the era of enormous population and vast industries, the power consumption of devices counts a major concern for both humans and the environment. This work is just an effort in conserving the power of devices. In this work, a serial communication protocol called Universal Asynchronous Receiver Transmitter (UART) is designed on Artix-7 Field Programmable Gate Array (FPGA). The implemented UART in this design work is a power-efficient UART, which is very much beneficial for green communication. The implementation work is done on the Xilinx 14.1 ISE Design Suite. To check the power consumption of UART, the voltage of the output load is varied from 1.0V to 3.0V. It is observed that the UART is the most power-efficient at 1.0V output voltage supply.

Keywords: *FPGA, UART, Xilinx, Voltage, Artix-7, Green Communication.*

1. Introduction

Data communication with a minimum amount of power utilization is one of the major issues that the world is facing. So people are moving towards the use of green communication and power-efficient devices [1-2]. This research work is done in order to promote and fulfill the ideas of green communication. In this work, a power-efficient UART device is implemented on Artix-7 FPGA. UART is Universal Asynchronous Receiver Transmitter which is used for serial communication [3]. UART requires the use of a single wire for both transmission of data and receiving of

data which is represented in figure 1 [4-5]. The UART requires no clock signals for transmitting data from transmitter end to receiver end.
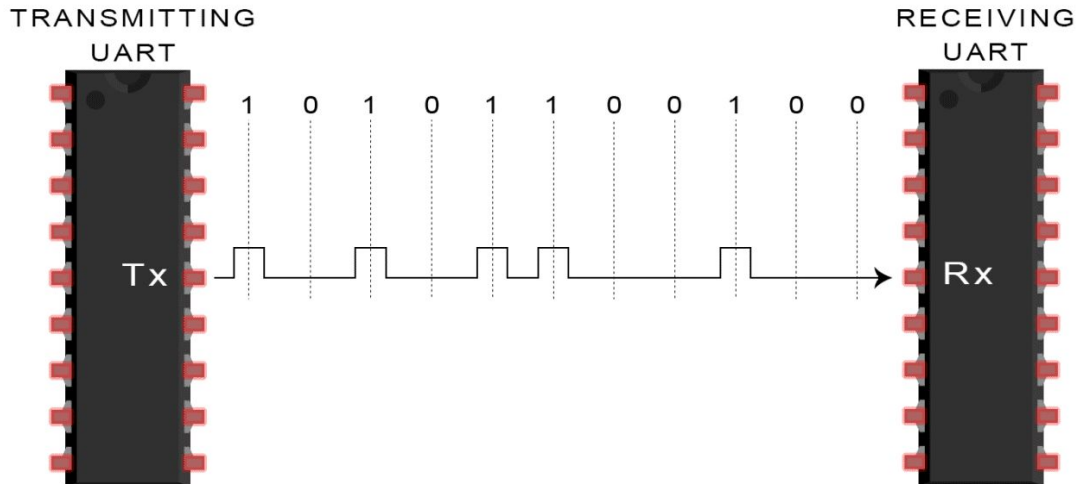
Fig 1. UART communication.

The proposed UART in this work is analyzed at different output load voltage value which is shown in figure 2.

Fig. 2 Different voltage value.

2. Related Work

Authors implemented a High-performance Random-Access Memory (RAM) design on 28 nm FPGA [6]. The power in this work is calculated for different LVCMOS I/O standards. A low power D Flip-Flop has been designed by authors using LVCMOS IO standards [7]. Researchers designed a green data flip-flop on FPGA using various LVCMOS I/O standards [8]. LVCMOS I/O standards based 4-bit register is implemented by researchers on FPGA [9]. Authors also designed an energy-efficient digital clock on Spartan-6 FPGA [10]. Clock gating-based an energy-efficient Arithmetic Logic Unit (ALU) is implemented on FPGA by researchers [11]. Therefore, a lot of work has been done for promoting green communication and power-efficient devices. But no work is done on power-efficient UART. So, in this work, a power-efficient UART is designed on Artix-7 FPGA.

3. Design Setup

The power-efficient UART is implemented on Xilinx 14.1 ISE Design Suite and the results of power consumptions are targeted on 28 nanometers (nm) Artix-7 FPGA. The power utilization of UART is done by the X Power Analyzer tool for the voltage range of 1.0V to 3.0V. The Register Transistor Level (RTL) of UART is described in figure 3. At the input side, there are nine-wire lines were as at the output side of UART there are four-wire lines.
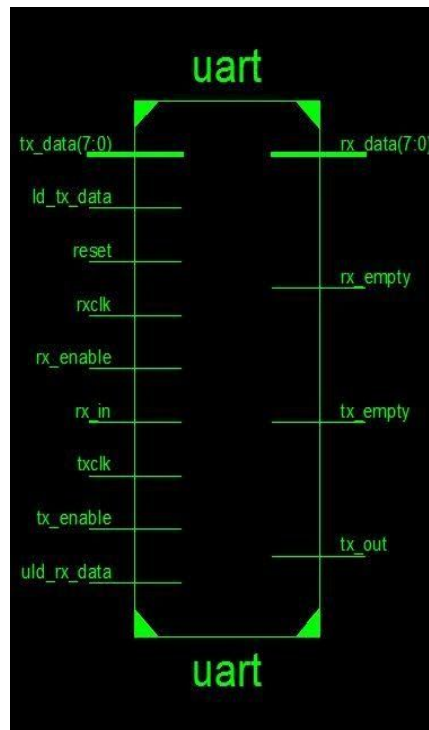

Fig. 3 RTL of UART.

4. Environmental Setup

The ambient temperature at which UART device is interfaced with Artix-7 FPGA is 250C with an airflow of 250 Linear Feet per Meter (LFM). The junction temperature of the UART is increased as the output voltage supply gets increased. The UART burns out, when the voltage supply reaches to 3V. The corresponding value of junction temperature with each value of voltage is illustrated in figure 4.
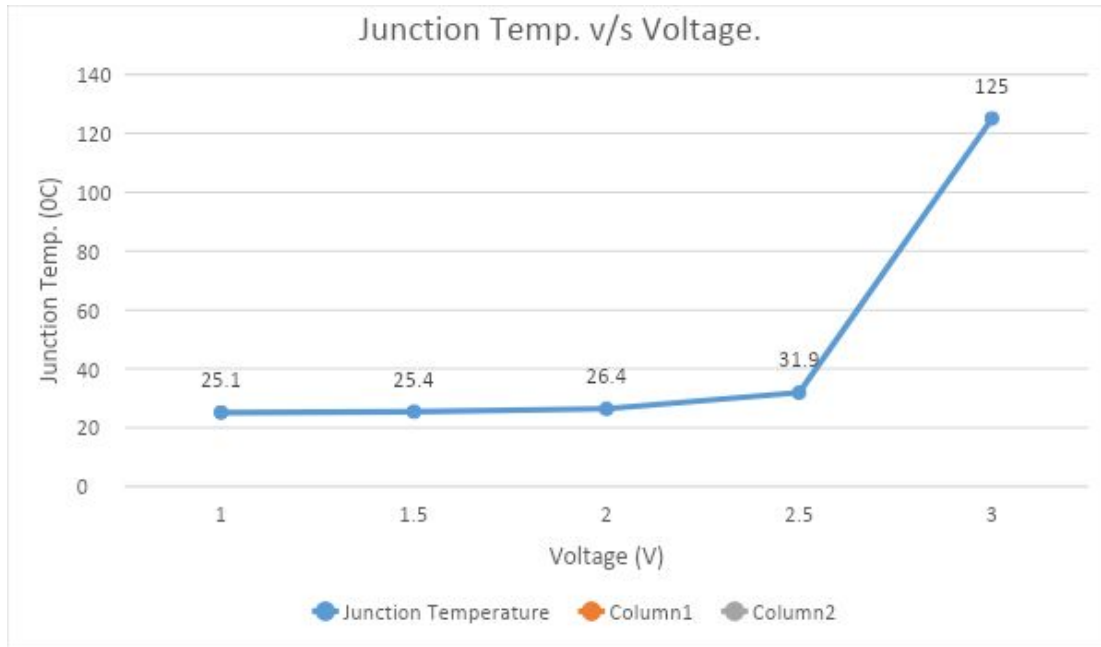

Fig. 4 Junction temperature v/s Voltage.

6. Power Calculation of UART with Artix-7 FPGA.

A. When the output voltage is 1.0V.

When the output voltage is at 1V there is only leakage power dissipation in the UART device which is 0.042W. All the other on-chips power of the device dissipates 0.00W of the power. Therefore the total power consumption of the device is also 0.042W. The power consumption of the UART device for 1V is described in table 1.

Table 1. Power consumption at $1.0V$.

On-chips	Power (W)
Clock	0.000
Logic	0.000
Signal	0.000

IOs	0.000
Leakage	0.042
Total	0.024

B. When the output voltage is 1.5V.

When the supply voltage of output load is scaled to 1.5V, the leakage power dissipation is 0.110W. The other on-chips power of the UART device contributes 0.00W power consumption. Therefore for 1.5V, the total power is 0.110W. The power consumption for 1.5V voltage is shown in table 2.

Table 2. Power consumption at $1.5V$.

On-chips	Power (W)
Clock	0.000
Logic	0.000
Signal	0.000
IOs	0.000
Leakage	0.110
Total	0.110

C. When the output voltage is 2.0V.

For the 2.0V output voltage. The total power and leakage power is same 0.419W. All the other on-chips power counts 0.000W power consumption in the total power consumption of the UART device which is shown in table 3.

Table 3. Power consumption at $2.0V$.

On-chips	Power (W)
Clock	0.000
Logic	0.000
Signal	0.000
IOs	0.000
Leakage	0.419
Total	0.419

D. When the output voltage is 2.5V.

When the output supply voltage of the UART device is tuned to 2.5V, the leakage power dissipation is 2.074 W, which is equal to the total power consumption of the device. There is 0.000W power consumption by all the other on-chips power of the UART device. Table 4, represents the power consumption for 2.5V voltage supply.

Table 4. Power consumption at $2.5V$.

On-chips	Power (W)
Clock	0.000
Logic	0.000
Signal	0.000
IOs	0.000
Leakage	2.074
Total	2.074

E. When the output voltage is 3.0V.

When the supply voltage of the output load is scaled up to 3.0V, the device gets burned. The total power consumption also reaches to the maximum value of 239.621W. The power consumption of the UART device for 3.0V is illustrated in table 5.

Table 5. Power consumption at $3.0V$.

On-chips	Power (W)
Clock	0.000
Logic	0.000
Signal	0.000
IOs	0.000
Leakage	239.621
Total	239.621[*]

*Red color denoted burning of device.

7. Results and Discussion

From the power analysis of the device, it is clearly observed that as the output voltage of the load increases the total power consumption of the device also increases. The device can be used up to the output voltage supply of 2.0V. When the voltage is tuned to 3.0V the device gets burned because of the heat. The total power comparison at different voltage levels is shown in figure 5.
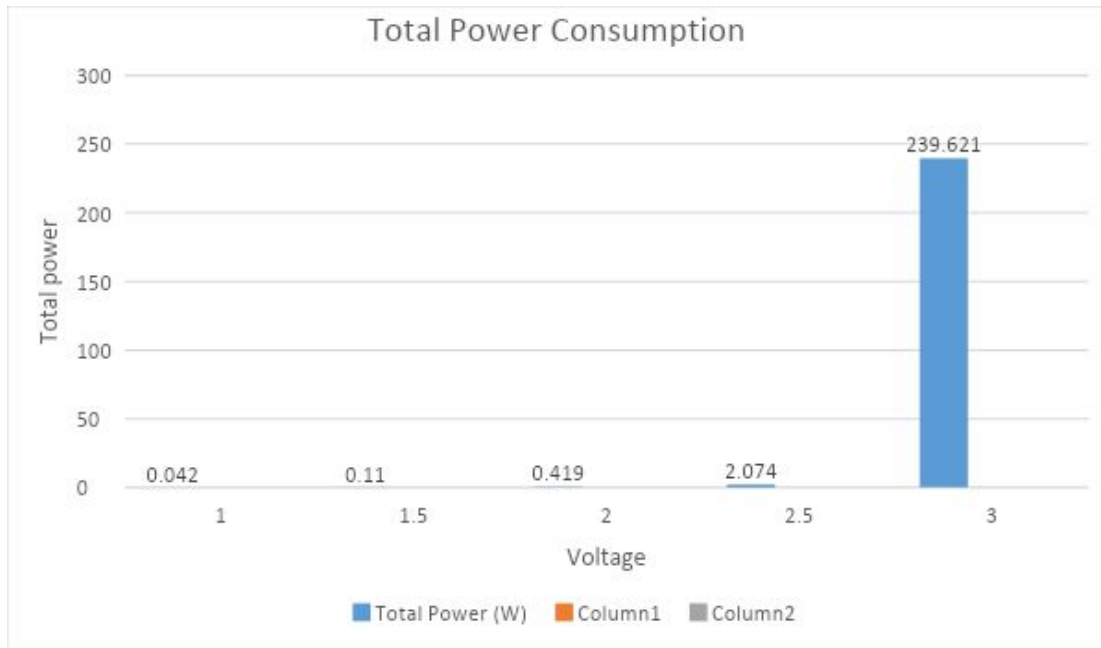
Fig. 5 Total power consumption at different voltage value.

8. Conclusion

In this work, a power-efficient UART device is implemented on 28nm Artix-7 FPGA. The implementation is done using Xilinx 14.1 ISE Design Suite. The power of the device increases as the output voltage increases, and when the voltage is scaled to 3.0V the device gets burned. The device can only use up to 2.0V of the output voltage. There is an increment of 161.9% of the total power consumption of the device, when the voltage change from 1.0V to 1.5V. There is an increment of 897.619% of the total power consumption of the device, when the voltage change from 1.0V to 2.0V. There is an increment of 6338.1% of the total power consumption of the device, when the voltage change from 1.0V to 2.5V. From the power analysis, it is clearly observed that the UART device is most power-efficient at 1.0V of the output voltage.

References

1. S. M T. Siddiquee, K. Kumar, B. Pandey, A. Kumar," Energy Efficient Instruction Register for Green Communication", International Journal of Engineering and Advanced Technology (IJEAT), Volume-8, Issue-2S2, January 2019.
2. K. Kumar, S. Ahmad, B. Pandey, A. K Pandit, D. Singh, D.M A.Hussain "Power Efficient Frequency Scaled and Thermal-Aware Control Unit Design on FPGA", International Journal of Innovative Technology and Exploring Engineering (IJITEE), Vol. 8, Issue-9S2, July 2019.

3. http://www.circuitbasics.com/basics-uart-communication/

4. K.Kumar, A.Kaur, B.Pandey, and S. N. Panda. "Low Power UART Design Using Different Nanometer Technology-Based FPGA." In 2018 8th International Conference on Communication Systems and Network Technologies (CSNT), pp. 1-3. IEEE, 2018.

5. K.Kumar, A. Kaur, S. N. Panda, and B. Pandey. "Effect of Different Nano Meter Technology-Based FPGA on Energy Efficient UART Design." In 2018 8th International Conference on Communication Systems and Network Technologies (CSNT), pp. 1-4. IEEE, 2018.

6. S. Bhalla, T. Kaur, K. Bansal, I. Ahuja, and S. Chawla. LVCMOS IO Standard Based High Performance RAM Design on 28nm FPGA. International Journal of Control and Automation, Vol. 9, no. 9, pp. 213-220, 2016.

7. T. Agrawal, et.al. LVCMOS Based Energy Efficient D flip-flop Design. 2nd International Conference on ISMAC (IoT in Social, Mobile, Analytics and Cloud) (ISMAC), 2018.

8. G. Gupta, A. Kaur, and B. Pandey. LVCMOS based Green Data Flip Flop Design on FPGA. Ninth International Conference on Advanced Computing (ICoAC), pp. 41-45, 2017.

9. T. Agrawal, A. Kumar, P. Aggarwal, and S. S. Tirmizi. LVCMOS Based 4-Bit Register. 9th International Conference on Computing, Communication and Networking Technologies (ICCCNT), 2018.

10. S. Pandey, et. al. Low Power Digital Clock Design Using LVCMOS Input/Output Standards on 45 nm FPGA. Gyancity Journal of Engineering and Technology, Volume 2, Issue 2, 2016.

11. B. Pandey, et.al. Clock gating based energy efficient ALU design and implementation on FPGA. International Conference on Energy Efficient Technologies for Sustainability, 2013.