Gyancity Journal of Engineering and Technology,
Vol.6, No.2, pp. 13-20, July 2020
ISSN: 2456-0065 DOI: 10.21058/gjet.2019.62002

Frequency Scaling Based FIR Filter Design

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Abstract

Energy efficiency, power consumption and heat dissemination are some of the most important factors considered in designing of a device's architecture. In this work, we have analyzed the resource utilization, availability and power consumption of FIR filter when implemented on four different FPGAs of 28nm and 16nm process technologies to determine the most energy efficient architecture. After the implementation of FIR filter on Kintex Ultrascale+ FPGA of speed grade -3 using LVCMOS 18 IO Standard, we have simultaneously analyzed the effect of changes in both airflow and heat sink on power consumption, junction temperature and thermal margin of the device when scaling frequency for different values like: 100GHz, 50GHz and 25GHz. We have used Xilinx Vivado 2018.2 ISE for all the observations done in this research work. Kintex Ultrascale+ FPGA is proved to be the most energy efficient FPGA because it has least power consumption, least utilization % and high availability of resources like LUT, FF, IO and BUFG. It is observed that the total on chip power, dynamic power, static power and junction temperature of the device decreases when airflow is increased from 250 LFM to 500 LFM and when the heat sink changes from Low profile to High profile. On scaling the frequency down from 100GHz to 50GHz, there is 48.3% reduction in total on chip power and 23.12% reduction in junction temperature of the device for airflow of 250 LFM and low heat sink profile. When frequency is scaled down from 100GHz to 25GHz there is 72.3% reduction in total on chip power and 34.58% reduction in junction temperature of the device for airflow of 250 LFM and low heat sink profile. For further enhancing the energy efficiency of FSM designed in this work, voltage scaling or clock gating can be applied to this device. Here we have only considered one IO standard, the power consumption of different IO Standards can be compared at different values of output load to increase efficiency of the device.

Keywords: *Airflow, Energy Efficient, FIR Filter, FPGA, Frequency scaling, Heat Dissemination, Heat Sink, Power Consumption*

1. Introduction

There are various types of digital filters. Finite impulse response (FIR) filter is one of them. It is called FIR because response to a unit impulse is finite in FIR filter [1]. The term digital filter arises because these filters operate on discrete-time signals. The term finite impulse response arises from the nature of the filter output which is

computed as a weighted, finite term sum, of past, present, and perhaps future values of the filter input. Due to their linear phase and inherent stability, variable bandwidth finite impulse response (FIR) filters are the popular choice in most of the applications. FIR filters are inherently stable because they don't have a feedback in its equation. Also, FIR filters can provide linear phases. Application of FIR filters although are mainly in digital signal processing applications, but are not limited or restricted to image processing, speech processing, digital audio but also in channel equalization, signal enhancement, and other communication areas [1]. The modern IT infrastructures have been extended and scaled, which brings various "green" related issues, such as energy consumption, heat dissemination, greenhouse emission, and resource total cost of ownership [2]. Frequency scaling and Thermal scaling are two of the Green Computing techniques. More processor chips generate more heat, more heat requires more cooling and cooling again generates heats and thus we come to a stage where we want to balance the system by getting the same computing speed at decreased energy consumption [3]. Therefore, in this work, we have first compared the utilization and power consumption of FIR filter on four different FPGAs like: Kintex Ultrascale+, Zynq Ultrascale+ MPSoC, Kintex-7 and Artix-7. Both Kintex Ultrascale+ and Zynq Ultrascale+ MPSoC are based on 16nm process technology but Artix-7 and Kintex-7 are based on 28nm process technology as shown in Table 1.

Table 1. Process Technology of FPGAs

FPGA	Device	Process Technology
Artix-7	xc7a12tcpg238-3	28nm
Kintex-7	xc7k70tfbg484-1	28nm
Zynq Ultrascale+ MPSoC	xczu4eg-fbvb900-3-e	16nm
Kintex Ultrascale+	xcku3p-ffva676-3-e	16nm

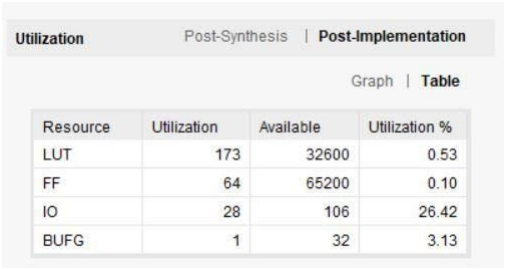
We have then implemented FIR filter on a 16nm Kintex Ultrascale+ FPGA with -3 speed grade using LVCMOS18 IO Standard. After implementation of FIR Filter, we have simultaneously analyzed the effect of airflow and heat sink on the junction temperature, thermal margin and power consumption of the FPGA when scaling frequency for different values like: 100GHz, 50GHz and 25GHz at constant output load. The mechanical structure of Heat Sink plays an important role to cool down the FPGA device [4]. Three types of different heat sink like: Low Profile, Medium Profile and High Profile are taken into consideration for this work. We have considered two different types of airflow; the slowest airflow is 250 LFM and the fastest airflow is 500 LFM. Airflow is useful in reducing heat dissipation of the device. The dynamics of airflow is defined in LFM (Linear Feet per Minute). Here we have used Xilinx Vivado 2018.2 ISE for all the observations and Verilog as the hardware description language.

2. Related Works

Voltage Scaling was used to design energy efficient Gaussian FIR Filter implemented on Kintex-7 FPGA [5]. Design and implementation of Energy aware Image ALU on FPGA is discussed in [6]. In [4], thermal scaling was performed on FIR filter design implemented on a 28nm FPGA. Digital filters with variable frequency response characteristics are required for numerous critical applications in the fields of digital communications, audio signal processing, biomedical signal processing etc. [7,8]. Scaling of output load from 5000 to 0 pF was carried out to show an effect of output load on both on-chip and off-chip power consumption of FIR filter design implemented on 20nm FPGA with the use of HSTL_II IO standards [9]. Energy efficient Finite Impulse Response (FIR) filter is widely used to increase working time of node of wireless sensor networks [10]. Our FIR design also delivers high performance.

3. Utilization of Resources on different FPGAs

Utilization and availability of resources of FIR filter on different FPGAs after implementation is shown in the following figures.

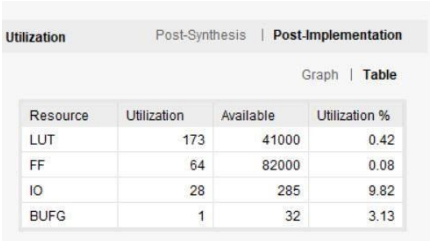

Utilization Post-Synthesis | Post-Implementation

Graph | Table

Resource	Utilization	Available	Utilization %
LUT	173	32600	0.53
FF	64	65200	0.10
IO	28	106	26.42
BUFG	1	32	3.13

Figure 1. Availability and Utilization of resource by FIR filter on Artix-7 FPGA

From Figure 1, the maximum utilization % is 26.42 for IO and minimum utilization % is 0.10 for FF in case of Artix-7.

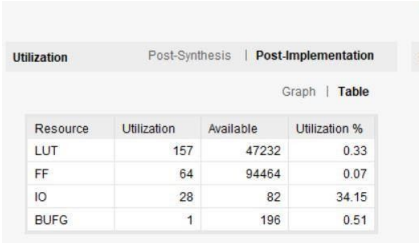

Utilization Post-Synthesis | Post-Implementation

Graph | Table

Resource	Utilization	Available	Utilization %
LUT	173	41000	0.42
FF	64	82000	0.08
IO	28	285	9.82
BUFG	1	32	3.13

Figure 2. Availability and Utilization of resource by FIR filter on Kintex-7 FPGA

From Figure 2, the maximum utilization % is 9.82 for IO and minimum utilization % is 0.08 for FF in case of Kintex-7.


Utilization Post-Synthesis | Post-Implementation

Graph | Table

Resource	Utilization	Available	Utilization %
LUT	157	47232	0.33
FF	64	94464	0.07
IO	28	82	34.15
BUFG	1	196	0.51

Figure 3. Availability and Utilization of resource by FIR filter on Zynq Ultrascale+ MPSoC FPGA

From Figure 3, the maximum utilization % is 34.15 for IO and minimum utilization % is 0.07 for FF in case of Zynq Ultrascale+ MPSoC.

Utilization — Post-Synthesis | Post-Implementation

Graph | Table

Resource	Utilization	Available	Utilization %
LUT	157	162720	0.10
FF	64	325440	0.02
IO	28	256	10.94
BUFG	1	256	0.39

Figure 4. Availability and Utilization of resource by FIR filter on Kintex Ultrascale+ FPGA

From Figure 4, the maximum utilization % is 10.94 for IO and minimum utilization % is 0.02 for FF in case of Kintex Ultrascale+. On comparing the utilization of resources by FIR filter for different FPGAs from Figure 1 to Figure 4, Kintex Ultrascale+ has the least utilization % for LUT, FF, IO and BUFG and Artix-7 has maximum utilization % for the same resources.

4. Power consumption by different FPGAs

Table 2. Power consumption of FIR filter on different FPGAs at output load of 0pF.

FPGAs	Total On Chip Power	Dynamic Power	Static Power
Artix-7	18.537 W	18.137 W	0.400 W
Kintex-7	18.302 W	18.092 W	0.210 W
Zynq Ultrascale+ MPSoC	28.923 W	28.049 W	0.874 W
Kintex Ultrascale+	14.646 W	13.976 W	0.670 W

According to the data in TABLE II, Kintex Ultrascale+ has the least total on chip power consumption that is 14.646W and Zynq Ultrascale+ MPSoC has the maximum total on chip power consumption that is 28.923W at output load of 0pF.

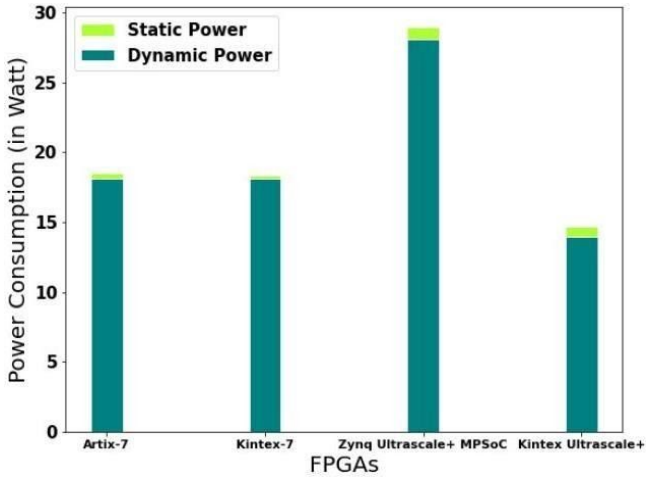


Figure 5. Power consumption by different FPGAs at output load of 0pF.

5. Varying Airflow and Heat Sink for different frequencies

Using 16nm Kintex Ultrascale+ FPGA for implementation of FIR filter, we have calculated its power consumption, junction temperature and thermal margin by simultaneously varying the values of airflow and heat sink at different frequencies, keeping output load constant at 0pF.

5.1 Power consumption at 100GHz

Table 3. Airflow of FPGA is 250 LFM

Heat Sink	Low	Middle	High
Total On Chip Power	12.671 W	12.615 W	12.593 W
Dynamic Power	12.029 W	12.029 W	12.029 W
Static Power	0.642 W	0.586 W	0.564 W
Junction Temperature	48.0 ^{0}C	42.7 ^{0}C	40.4 ^{0}C
Thermal Margin	52 .0 ^{0}C	57.3 ^{0}C	59.6 ^{0}C

At 100 GHz frequency and airflow of 250LFM, the total on chip power decreases from 12.671W to 12.593W and junction temperature decreases from 48.0 ^{0}C to 40.4 ^{0}C as the heat sink is varied from low to high. The thermal margin increases from 52.0 ^{0}C to 59.6 ^{0}C for the same.

Table 4. Airflow of FPGA is 500 LFM

Heat Sink	Low	Middle	High
Total On Chip Power	12.615 W	12.580 W	12.568 W
Dynamic Power	12.029 W	12.029 W	12.029 W
Static Power	0.586 W	0.551 W	0.539 W
Junction Temperature	42.8 ^{0}C	38.9 ^{0}C	37.3 ^{0}C
Thermal Margin	57.2 ^{0}C	61.1 ^{0}C	62.7 ^{0}C

At 100 GHz frequency and airflow of 500 LFM, the total on chip power decreases from 12.615W to 12.568W and junction temperature decreases from 42.8 ^{0}C to 37.3^{0}C as the heat sink is varied from low to high. The thermal margin increases from 57.2 ^{0}C to 62.7 ^{0}C for the same.

5.2 Power consumption at 50GHz

Table 5. Airflow of FPGA is 250 LFM

Heat Sink	Low	Middle	High
Total On Chip Power	6.550 W	6.530 W	6.522 W
Dynamic Power	6.015 W	6.015 W	6.015 W
Static Power	0.535 W	0.515 W	0.507 W
Junction Temperature	36.9 ^{0}C	34.2 ^{0}C	33.0 ^{0}C
Thermal Margin	63.1 ^{0}C	65.8 ^{0}C	67.0 ^{0}C

At 50 GHz frequency and airflow of 250 LFM, the total on chip power decreases from 6.550W to 6.522W and junction temperature decreases from 36.9 ^{0}C to 33.0 ^{0}C

as the heat sink is varied from low to high. The thermal margin increases from 63.1 ^{0}C to 67.0 ^{0}C for the same.

Table 6. Airflow of FPGA is 500 LFM

Heat Sink	Low	Middle	High
Total On Chip Power	6.530 W	6.517 W	6.512 W
Dynamic Power	6.015 W	6.015 W	6.015 W
Static Power	0.516 W	0.503 W	0.497 W
Junction Temperature	34.2 ^{0}C	32.2 ^{0}C	31.4 ^{0}C
Thermal Margin	65.8 ^{0}C	67.8 ^{0}C	68.6 ^{0}C

At 50 GHz frequency and airflow of 500 LFM, the total on chip power decreases from 6.530W to 6.512W and junction temperature decreases from 34.2 ^{0}C to 31.4 ^{0}C as the heat sink is varied from low to high. The thermal margin increases from 65.8 ^{0}C to 68.6 ^{0}C for the same.

5.3 Power consumption at 25GHz

Table 7. Airflow of FPGA is 250 LFM

Heat Sink	Low	Middle	High
Total On Chip Power	3.504 W	3.496 W	3.492 W
Dynamic Power	3.007 W	3.007 W	3.007 W
Static Power	0.497 W	0.489 W	0.485 W
Junction Temperature	31.4 ^{0}C	29.9 ^{0}C	29.3 ^{0}C
Thermal Margin	68.6 ^{0}C	70.1 ^{0}C	70.7 ^{0}C

At 25 GHz frequency and airflow of 250 LFM, the total on chip power decreases from 3.504W to 3.492W and junction temperature decreases from 31.4 ^{0}C to 29.3 ^{0}C as the heat sink is varied from low to high. The thermal margin increases from 68.6 ^{0}C to 70.7 ^{0}C for the same.

Table 8. Airflow of FPGA is 500 LFM

Heat Sink	Low	Middle	High
Total On Chip Power	3.496 W	3.490 W	3.488 W
Dynamic Power	3.007 W	3.007 W	3.007 W
Static Power	0.489 W	0.483 W	0.480 W
Junction Temperature	29.9 ^{0}C	28.8 ^{0}C	28.4 ^{0}C
Thermal Margin	70.1 ^{0}C	70.2 ^{0}C	71.6 ^{0}C

At 25 GHz frequency and airflow of 500 LFM, the total on chip power decreases from 3.496W to 3.488W and junction temperature decreases from 29.9 ^{0}C to 28.4 ^{0}C as the heat sink is varied from low to high. The thermal margin increases from 70.1 ^{0}C to 71.6 ^{0}C for the same.

6. Conclusion

16nm Kintex Ultrascale+ FPGA is proved to be the most energy efficient FPGA because it has comparatively least power consumption, least utilization % and high availability of resources like LUT, FF, IO and BUFG. It is observed that the total on chip power, dynamic power, static power and junction temperature of the device decreases when simultaneously airflow is increased from 250 LFM to 500 LFM and heat sink changes from Low profile to High profile. The power consumption and junction temperature of the device at any frequency is maximum for the device setting of 250 LFM airflow and low profile heat sink. When frequency is scaled down from 100GHz to 50GHz, there is 48.3% reduction in total on chip power and 23.12% reduction in junction temperature of the device airflow of 250 LFM and low heat sink profile. When frequency is scaled down from 100GHz to 25GHz there is 72.3% reduction in total on chip power and 34.58% reduction in junction temperature of the device for airflow of 250 LFM and low heat sink profile.

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Authors

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Anjali Sharma has completed her first bachelor's degree in Sciences and now she is a student of Computer science and pursuing Bachelor of Technology at Birla Institute of Applied Sciences. She has done a paper work on the technology that will provide benefits to the new generation as, her aim was to develop the technology that can be sustained without being damaging the

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Vaishnavi Bisht is starting her third year at Birla Institute of Applied Sciences, Bhimtal, India where she is pursuing Bachelor of Technology in Computer Science. She has earlier worked on a research paper under the guidance of her professor Dr. Bishwajeet Pandey which has been accepted in 12th IEEE CICN conference 2020. Her interest in data visualization and machine intelligence began when she came across Refik Anadol's work. She aspires to pursue a career in data visualization to find ways by which it can be integrated with artificial intelligence.